

**NEW
DATA
UPDATE 11**

**NATIONAL
SEMICONDUCTOR
CORPORATION**



AUGUST 1984



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A handwritten signature in cursive script, reading 'Charles E. Sporck'.

Charles E. Sporck
President, Chief Executive Officer
National Semiconductor Corporation

NEW DATA UPDATE 11

NATIONAL SEMICONDUCTOR CORPORATION

The New Data Update 11 is provided by National Semiconductor in order to keep you abreast of the latest products available. This special issue features the first pages of data sheets published February 1984 through July 1984 (two quarters). Two alpha-numerical indexes, one by device number and one by device function, serve as guides to the contents of this Update. A third index provides a listing of new application notes and briefs. These indexes/tables of contents are located in the front of the book. One additional index serves as an ordering guide for all other application notes and briefs which are still available (this index is located in the back of the book).

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TABLE OF CONTENTS/INDEX

BY DEVICE NUMBER:

	UPDATE NUMBER		UPDATE NUMBER
ADC0811 8-Bit Serial I/O A/D Converter with 11-Channel MUX.....	100576	LM2889 TV Video Modulator.....	107967
ADC0829 μ P Compatible 8-Bit A/D with 11-Channel MUX.....	100590	LM3361A Low Voltage Power Narrow Back- ground FM-IF System.....	108090
ADC1001, ADC1021 10-Bit μ P Compatible A/D Converters.....	100600	LMC835 Digital Controlled Graphic Equalizer.....	108465
ADC1210, ADC1211 12-Bit CMOS A/D Converters.....	100601	LP339 Ultra-Low Power Comparator.....	108490
BLC™-86/30 Board Level Computer.....	101514	MM58146 TV Clock and Channel Display.....	111290
BLX™-218 Floppy Disk Controller.....	101550	MM58241 High Voltage Display Driver.....	111392
DAC1265A, DAC1265 Hi-Speed 12-Bit D/A Converter with Reference.....	102398	MM58274 Microprocessor Compatible Real- Time Clock.....	111462
DH0011A High Voltage High Current Driver.....	102460	MM58341 High Voltage Display Driver.....	111422
DM77/87SR27, DM77/87SR27B (512x8) 4K-Bit Registered TTL PROM.....	102861	NMC27C58 8, 192-Bit (1024x8) UV Erasable CMOS PROM.....	112263
DM77/87SR25, DM77/87SR476B, DM77/87SR25B (512x8) 4K-Bit Registered TTL PROM.....	102660	NMC9345 1024-Bit Serial Electrically Erasable Programmable Memory (5V Only).....	102460
DS8910 AM-Only Digital Phase-Locked Loop Frequency Synthesizer.....	103660	NSC810A RAM-I/O-Timer.....	112711
ECL Programmable Array Logic (PAL®) Family.....	114400	PAL20A2 Programmable Array Logic (PAL®) Low Power PAL Series 20A2.....	114403
LH0132 Ultra-Fast FET Input Operational Amplifier.....	106402	PAL20B Programmable Array Logic (PAL®) Ultra-High Speed PAL Series 20B.....	114407
LM133/LM333/LM333A 3-Ampere Adjustable Negative Regulators.....	106489	Programmable Array Logic Family Series 24A.....	114402
LM592/LM592A Differential Video Amp.....	107150	SCX6260 CMOS Gate Array.....	113588
LM832 Dynamic Noise Reduction System™.....	107249	SYS32™ Multi-User Development System for the Series 32000™ Microprocessor Family.....	113645
LM833 Dual Audio Operational Amplifier.....	107280	TP3064, TP3067 Monolithic Serial Interface CMOS CODEC/Filter COMBOS.....	113978
LM1014 Motor Speed Regulator.....	107283		
LM1837 Low Noise Preamplifier for Auto Reversing Tape Playback Systems.....	107537		

TABLE OF CONTENTS/INDEX

BY DEVICE FUNCTION:

	UPDATE NUMBER		UPDATE NUMBER
A/D, D/A CONVERTERS		GATE ARRAYS	
ADC0829 μ P Compatible 8-Bit A/D with 11-Channel MUX	100590	SCX6260 CMOS Gate Array	113588
ADC1210, ADC1211 12-Bit CMOS A/D Converters	100601	MICROPROCESSORS	
DAC 1265A, DAC1265 Hi-Speed 12-Bit D/A Converter with Reference	102398	NSC810A RAM-I/O-Timer	112711
AMPLIFIERS		MONOLITHIC	
ADC1001, ADC1021 10-Bit μ P Compatible A/D Converters	100600	TP3064, TP3067 Monolithic Serial Interface CMOS CODEC/Filter COMBOS	113978
LH0132 Ultra-Fast FET Input Operational Amplifier	106402	PALS	
LM833 Dual Audio Operational Amplifier	107280	ECL Programmable Array Logic (PAL [®]) Family	114400
AUDIO		PAL20A2 Programmable Array Logic (PAL [®]) Low Power PAL Series 20A2	114403
LM832 Dynamic Noise Reduction System™	107249	PAL20B Programmable Array Logic (PAL [®]) Ultra High Speed PAL Series 20B	114407
LMC835 Digital Controlled Graphic Equalizer	108465	PAL24A Programmable Array Logic Family Series 24A	114402
LM1837 Low Noise Preamplifier for Auto Reversing Tape Playback Systems	107537	PHASE-LOCKED LOOP FREQUENCY SYNTHESIS	
BOARD LEVEL COMPUTER AND DEVELOPMENT SYSTEMS		DS8910 AM-Only Digital Phase-Locked Loop Frequency Synthesizer	103660
BLC86/30 Board Level Computer	101514	RADIO	
BLX218 Floppy Disk Controller	101550	LM3361A Low Voltage/Power Narrow Band FM-IF System	108090
SYS32™ Multi-User Development System for the Series 32000™ Microprocessor Family	113645	TACHOMETERS	
CLOCKS		LM1014 Motor Speed Regulator	107283
MM58274 Microprocessor Compatible Real-Time Clock	111462	VIDEO	
COMBINED FUNCTION ANALOG SWITCHES		LM2889 TV Video Modulator	107967
ADC0811 8-Bit Serial I/O, A/D Converter with 11-Channel Multiplexer	100576	VOLTAGE COMPARATORS/REGULATORS	
DISK SUPPORT		LM133/LM333/LM333A 3-Ampere Adjust- able Negative Regulators	106489
LM592/LM592A Differential Video Amp	107150	LP339 Ultra-Low Power Comparator	108490
DISPLAYS/DISPLAY DRIVERS			
DH0011A High Voltage High Current Driver	102460		
MM58146 TV Clock and Channel Display	111290		
MM58241 High Voltage Display Driver	111392		
MM58341 High Voltage Display Driver	111422		
EEPROMs/ROMs			
DM77/87SR476	102660		
NMC27C58 8, 192-Bit (1024x8) UV Erasable CMOS PROM	112263		
NMC9345 1024-Bit Serial Electrically Erasable Programmable Memory (5V only)	102460		
DM77/87SR27, DM77/87SR27B (512x8) 4-K-Bit Registered TTL PROM	102861		

INDEX OF NEW APPLICATION NOTES AND BRIEFS

ORDER NUMBER	APPLICATION NOTES	APPLICATION DATE
100350	AN-350 Designing An LCD Dot Matrix	February 1984
100353	AN-353 MM58167A Real-Time Clock Design Guide	May 1984
100354	AN-354 TMP Row and Attribute Table Lookup Operation	February 1984
100355	AN-355 TMP Dynamic RAM Interfacing	March 1984
100358	AN-358 NS80504 Microwave Plus Interface	April 1984
100359	AN-359 The MM58174A Real-Time Clock in a Battery Backed-up Design	February 1984
100360	AN-360 An Auto-Error Correction	February 1984
100361	AN-361 High Performance TTL Compatible Macrocell Arrays	May 1984
100365	AN-365 The MM58274 Adds Reliable Real-Time Keeping	April 1984
100367	AN-367 TMP External Character Generation	February 1984
100368	AN-368 An Introduction and Com- parison of 54HCT/74HCT	March 1984
100369	AN-369 NS455 TMP Logic Analyzer	May 1984

ORDER NUMBER	APPLICATION BRIEFS	APPLICATION DATE
114521	AB 12 Wide Adjustable Range PNP Voltage Regulator	February 1984
114522	AB 13 Avoid Problems Caused by Capacitive Coupling	May 1984
114523	AB 14 Throughput Considerations in NS455	February 1984
114524	AB 15 Protecting Data in the NMC9306	May 1984
114525	AB 16 NS455-Series TMP External Interrupt Processing	May 1984

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ADVANCED BIPOLAR LOGIC DATABOOK

The Advanced Bipolar Logic Databook contains the most current information available from National Semiconductor on the Advanced Schottky and Advanced Low Power Schottky families.

Both the DM54/74ALS and DM54/74AS families are designed to meet the systems designer's needs. The ALS family of devices has very low power requirements in addition to a higher low level threshold than LS and speed improvements over LS. The AS family provides the ultimate in speed as well as significant reductions in power dissipation over present Schottky. Both families offer $\pm 10\% V_{CC}$ over the military and commercial full temp range as standard product to facilitate maximum design flexibility and elimination of special drawings. Both of these advanced logic families are in their early production phases and will be continually expanded in future publications. For more information on either of these families, contact your National Semiconductor representative.

Page Count: 240 Price: \$5.00 Year: 1982

ADVANCED SCHOTTKY DATABOOK

The DM54/74AS family of devices is designed to meet the needs of system designers who require the ultimate in speed. AS achieves the fastest prop delays bipolar technology can offer (2 ns per gate). The AS family also offers significant reduction in power dissipation (8 mW per gate) over present Schottky (54/74S) with toggle rate capability of up to 200 MHz.

The AS family is TTL pinout compatible and offers Schottky (54/74S) drive capability with better fanout, higher noise immunity and faster operation.

For maximum design flexibility and elimination of special drawings, the AS family will be introduced with $\pm 10\% V_{CC}$ over the military and commercial full temp range as standard product. Furthermore, all switching characteristics are guaranteed over the full temperature and V_{CC} range.

Page Count: 172 Price: \$5.00 Year: 1982

CMOS DATABOOK - 1981

The CMOS Databook describes National Semiconductor's standard SSI/MSI CMOS products. This includes the 54C/74C-Series logic family, which is equivalent to the 7400 family of TTL devices.

Also described are CD40XXB and CD45XXB-Series devices. Specifications for special function, LSI, A/D converters and memory devices are provided, offering the designer unique high density low power system solutions.

Page Count: 928 Price: \$6.00 Year: 1981

CMOS DATABOOK - 1984

The CMOS Databook contains the industry's most comprehensive collection of high-performance CMOS products available. Our early commitment to micro-CMOS technology has made possible the development of a broad spectrum of advanced devices that will simplify your design and ensure state-of-the-art systems.

microCMOS technology describes National's array of small-geometry, silicon gate, oxide-isolated processes used to build the products in this book. Using N- or P-well substrates and multiple-layer metal or polysilicon-interconnect structures, microCMOS processes feature sizes of 3.0, 2.0 or 1.5 microns, with submicron feature sizes in development.

Page Count: 1520 Price: \$12.00 Year: 1984

COPS MICROCONTROLLERS DATABOOK

The COPS Microcontrollers Databook offers the most current information available from National Semiconductor on the COPS microcontroller family. Included in this publication are sections on: single-chip, ROMless and piggyback microcontrollers, standard controllers, MICROWIRE peripherals, EPROMs and support circuits, and development systems and user's manuals, as well as the applications for these products.

COPS products offer cost efficiency and design flexibility as well as development ease, and will be continually upgraded and expanded. Continue to look for future databooks providing information on new developments which may improve your capability to bring your ideas to market.

For more information, contact your National Semiconductor representative concerning any of our COPS family products.

Page Count: 834 Price: \$6.00 Year: 1982

DATA CONVERSION/ACQUISITION DATABOOK

The 1984 edition of the Data Conversion/Acquisition Databook is one of the most comprehensive in the industry. It contains specifications for high technology conversion products in the analog signal path, both preceding and following the conversion process.

Combining high volume production capability with leading edge technology such as thin film resistors, laser trimming and advanced microCMOS and bipolar processing, has helped develop products best suited to your design needs.

Page Count: 1232 Price: \$12.00 Year: 1984

48-SERIES MICROPROCESSOR HANDBOOK

This handbook contains detailed design-related information pertaining to the National Semiconductor 48-Series single-chip microcomputers and microprocessors.

The material presented is at a level of detail to aid in the design and development of systems using the 48-Series microcomputers.

Topics include the 48-Series architecture, expansion, and instruction set.

Additional hardware examples, integrated with the required software, and various data sheets of compatible devices are given.

Page Count: 192 Price: \$5.00 Year: 1980

HYBRID PRODUCTS DATABOOK

The Hybrid Products Databook is the only National Semiconductor publication that contains complete information on all of our hybrid semiconductor products.

Included are precision thin film and thick film products which provide the user with standard functions from operational amplifiers to converters with capabilities beyond those of current monolithic technology.

Product selection guides and an application section are also included.

Page Count: 792 Price: \$7.00 Year: 1982

INTERFACE BIPOLAR LSI/BIPOLAR MEMORY/PROGRAMMABLE LOGIC DATABOOK

This databook provides complete specifications for a variety of transmission line drivers/receivers, peripheral/power drivers, and level translators/buffers.

Product selection guides list applications information and operating features. Memory, dynamic memory, microprocessor, data communications, and disk support products are also covered in the databook.

The interface appendices section contains cross reference guides; the programmable logic section describes the technology, design, and gives application suggestions.

Page Count: 1520 Price: \$12.00 Year: 1983

INTUITIVE IC OP AMPS DATABOOK

This book targets some of the most significant transitions in semiconductor technology since the change from germanium silicon.

Intuitive IC CMOS Evolution highlights the transition in the reduction in defect densities and the development of new circuit topologies.

Page Count: 299 Price: \$12.95 Year: 1984

LINEAR DATABOOK

The 1982 edition of the National Semiconductor Linear Databook is the most comprehensive available. It presents approximately 2000 pages of specifications for our high-technology linear products. Applications, descriptions, features and diagrams in this databook include detailed sections for Voltage Regulators, Op Amps, Voltage Comparators, A to D, D to A Converters, Industrial Blocks and Audio, and TV Circuits.

The databook also features advanced telecommunication devices and speech synthesis (DIGITALKER®), plus other non-state-of-the-art linear products offering performance, economy, quality and reliability.

Page Count: 1952 Price: \$12.00 Year: 1982

MOS MEMORY DATABOOK

The 1984 MOS Memory Databook is a comprehensive collection of information advanced, high-density memory products covering the spectrum of this mainstream semiconductor component category.

National Semiconductor has an array of advanced technology processes to apply to memory design and development. These range from high-density triple-poly process used in the most advanced RAMs, the small-geometry, silicon gate, oxide-isolated micro-CMOS technology which is now being applied to high-performance memory devices for the first time.

Page Count: 256 Price: \$6.00 Year: 1984

NS16000 DATABOOK

This 500-page databook includes specs, instruction sets and architectural descriptions of the three CPU families: (NS08032, NS16032 and NS32032); plus memory management, floating point, and 10 peripherals.

Also featured is information on the supporting development tools and software—the SYS16, ISE/16, DB16000, cross software, and GENIX operating system.

GENIX, a version of Berkeley 4.1 bsd UNIX tailored for the NS16000 family, supports Demand Paged Virtual Memory and optimizes the NS16000 architectural elegance. GENIX runs on SYS16 and is available in source code form for OEM adaptation to NS16000-based systems.

Page Count: 280 Price: \$7.00 Year: 1983

PAL® DATABOOK

This book is intended to be a complete reference for the design of digital systems using Programmable Array Logic (PAL) devices. In addition to data sheets for all currently available devices, this book also contains extensive application notes intended to give design examples for a number of PAL devices. It also contains a step-by-step procedure for PAL design and programming, including the listing for PALASM®, which is a FORTRAN IV program that converts logic equations to PAL programming information.

Portions of this book have been reprinted with the permission of Monolithic Memories Inc., the originator of the PAL concept.

Page Count: 176 Price: \$6.00 Year: 1982

RELIABILITY HANDBOOK VOLUME I

The Reliability Handbook Volume I penetrates the barrier of technical jargon and procedural ritual that has grown around the subject of semiconductor reliability, enabling the reader to clearly understand the areas that directly concern the application of semiconductors within the Military/Aerospace electronic systems.

This handbook focuses on areas of concern to all users of semiconductors where device reliability is of paramount importance. It examines the devices themselves and discusses the most widely accepted and specific test procedures designed to test reliability. Throughout, the relationship of electrical, mechanical, environmental, and visual tests and inspections to the nature of the devices is emphasized. Discussions include the MIL-STD-883, MIL-M-38510, VLSI/VHSIC, 883B/RETS™, 883S/RETS™.

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Page Count: 285 Price: \$7.00 Year: 1982

TRANSISTOR DATABOOK

National Semiconductor has added many new transistors and product families since publication of the last databook. Many have already been widely acclaimed by users.

In addition to small-signal, power-bipolar and field-effect transistors that have been the mainstay of our catalog, there is a section for multiple-field-effect transistors. More part numbers will be added as market needs expand.

To keep current on all new National transistors, please contact your National sales representative or franchised distributor and ask to be placed on the customer mailing list.

Page Count: 558 Price: \$6.00 Year: 1982

VOLTAGE REGULATOR HANDBOOK

With the variety of fixed- and variable-regulator technology currently available, the 336-page Voltage Regulator Handbook becomes a must for the selection of three-terminal and dual tracking components that meet the system requirement while utilizing the most cost-effective approach.

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100022	AN-22 ICs for Digital Data Transmission
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100159	AN-159 Data Acquisition System Interface to Computers
100252	AN-252 Speech Synthesis
100254	AN-254 Expanding 48-Series Program Space in 4k Byte Increments
100256	AN-256 Circuitry for Inexpensive Relative Humidity Measurement
100257	AN-257 Simplified Multi-Digit LED Display Design Using MM74C911/MM74C912/MM74C917 Display Controllers
100259	AN-259 DS3662, the Bus Optimizer
100263	AN-263 Sine Wave Generation Techniques
100269	AN-269 Circuit Applications of Multiplying CMOS D-to-A Converters
100271	AN-271 Applying the New CMOS Micro-DACS™
100272	AN-272 Op Amp Booster Designs
100278	AN-278 Designing with a New Super-Fast Dual Norton Amplifier
100280	AN-280 A/D Converters Easily Interface with 70-Series Microprocessors
100281	AN-281 Data Acquisition Using INS8048
100282	AN-282 INS8048 Display Driver Interface
100283	AN-283 INS8070 Multiprocessing Systems Programming
100285	AN-285 An Acoustic Transformer Powered Super-High Isolation Amplifier
100286	AN-286 Applications of the LM392 Comparator Op Amp IC
100287	AN-287 Voice Recording Techniques for Speech Synthesis
100288	AN-288 System-Oriented DC-DC Conversion Techniques
100289	AN-289 Circuit Applications of Analog Data Multiplexers
100290	AN-290 Application of the MM53200 Encoder/Decoder
100293	AN-293 Control Applications of CMOS DACs
100294	AN-294 Special Sample and Hold Techniques
100295	AN-295 A High Performance Industrial Weighing System
100296	AN-296 Crystal/INS8048 Oscillator
100297	AN-297 NS80CX48 Extra Features
100298	AN-298 Isolation Techniques for Signal Conditioning
100300	AN-300 Simple Circuit Detects Loss of 4-20 mA Signal
100303	AN-303 HC-CMOS Power Dissipation
100307	AN-307 Introducing the MF10: A Versatile Monolithic Active Filter Building Block
100310	AN-310 High-Speed CMOS (MM54HC/MM74HC) Processing

ORDER NUMBER APPLICATION NOTES

100311	AN-311 Theory and Applications of Logarithmic Amplifiers
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100313	AN-313 DC Electrical Characteristics of MM54HC/MM74HC High-Speed CMOS Logic
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100316	AN-316 The Subscriber Line Card in a Distributed Control Switching System
100317	AN-317 AC Characteristics of MM54HC/MM74HC High-Speed CMOS
100319	AN-319 Comparison of MM54HC/MM74HC to 54LS/74LS and ALS
100320	AN-320 A 2.4k CMOS Gate Array
100321	AN-321 Gate Array and Custom VLSIC Fabrication with the microCMOS Process
100322	AN-322 A 2.4k microCMOS Gate Array System Design Facility
100323	AN-323 A Manchester-Coded Fiber-Optic Serial Data Link Interfacing Parallel Data Buses at Data Rates to 200k Bytes/Sec
100324	AN-324 Microcontroller Implementation of an Intelligent, Full Duplex, 300 Baud Modem
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100328	AN-328 EEPROM Application Note V _{pp} Generation On Board
100329	AN-329 Implementing an 8-Bit Buffer in COPS
100330	AN-330 How to Use a COP420R/COP444LR
100331	AN-331 SCX Family microCMOS Gate Array System Cost Analysis
100332	AN-332 1.2k CMOS Gate Array
100333	AN-333 On-Chip Memory and Test Functions for Gate Arrays
100338	AN-338 Designing with the NMC9306/COP494 a Versatile Simple to Use E ² PROM
100339	AN-339 National's Process Enhancements Eliminate the CMOS SCR Latch-Up Problem in 54HC/74HC Logic
100341	AN-341 Time-Domain Synthesis Gives Good-Quality Speech at Very Low Data Rates
100342	AN-342 Designing with the NMC9817, a 2nd Generation E ² PROM
100343	AN-343 LH1605 Switching Regulator
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100349	AN-349 CMOS 300 Baud Modem

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114490	AB 1 DP8408, DP8409 Application Hints
114493	AB 3 Current Consumption in NMOS COPS Microcontrollers
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ADC0811 8-Bit Serial I/O A/D Converter With 11-Channel Multiplexer

General Description

The ADC0811 is an 8-Bit successive approximation A/D converter with simultaneous serial I/O. The serial input controls an analog multiplexer which selects from 11 input channels or an internal half scale test voltage.

An input sample-and-hold is implemented by a capacitive reference ladder and sampled data comparator. This allows the input signal to vary during the conversion cycle.

Separate serial I/O and conversion clock inputs are provided to facilitate the interface to various microprocessors.

Features

- Separate asynchronous converter clock and serial data I/O clock.
- 11-Channel multiplexer with 4-Bit serial address logic.
- Built-in sample and hold function.

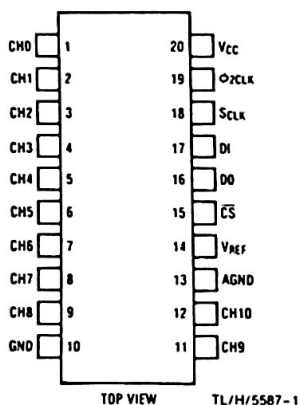
- Ratiometric or absolute voltage referencing.
- No zero or full-scale adjust required.
- Internally addressable test voltage.
- 0V to 5V input range with single 5V power supply.
- T2L/MOS input/output compatible.
- 0.3" standard width 20-pin dip or 20-pin molded chip carrier

Key Specifications

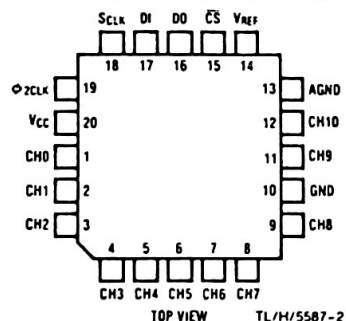
- | | |
|--------------------------|---|
| ■ Resolution | 8-Bits |
| ■ Total unadjusted error | $\pm \frac{1}{2}\text{LSB}$ and $\pm 1\text{LSB}$ |
| ■ Single supply | 5V _{DC} |
| ■ Low Power | 15 mW |
| ■ Conversion Time | 32 μS |

Connection Diagrams

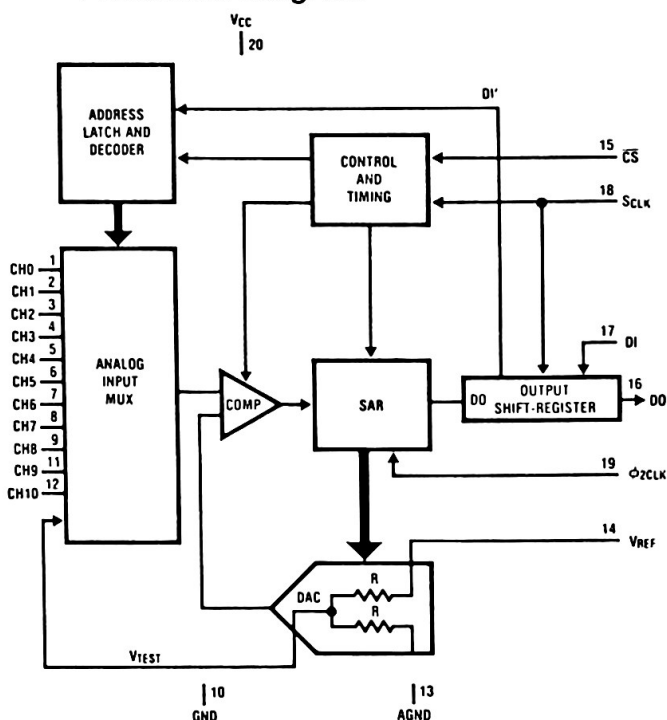
Dual-In-Line Package



Molded Chip Carrier (MCC) Package



Functional Diagram



ADC0829 μ P Compatible 8-Bit A/D with 11-Channel MUX/Digital Input

General Description

The ADC0829 is an 8-bit successive approximation A/D converter with an 11-channel multiplexer of which six can be used as digital inputs, as well as, analog inputs.

This A/D is designed to operate from the μ P data bus using a single 5V supply.

Channel selection, conversion control, software configuration and bus interface logic are all contained on this monolithic CMOS device.

This device contains three 16-bit registers which are accessed via double byte instructions. The control register is a write only register which controls the start of a new conversion, selects the channel to be converted, configures the 8-bit I/O port as input or output, and provides information for the 8-bit output register.

The conversion results register is a read only register which contains the current status and most recent conversion results. The discrete input register is also a read only register which contains the four address bits of the selected channel, and the six discrete inputs which are connected to the analog multiplexer.

Key Specification

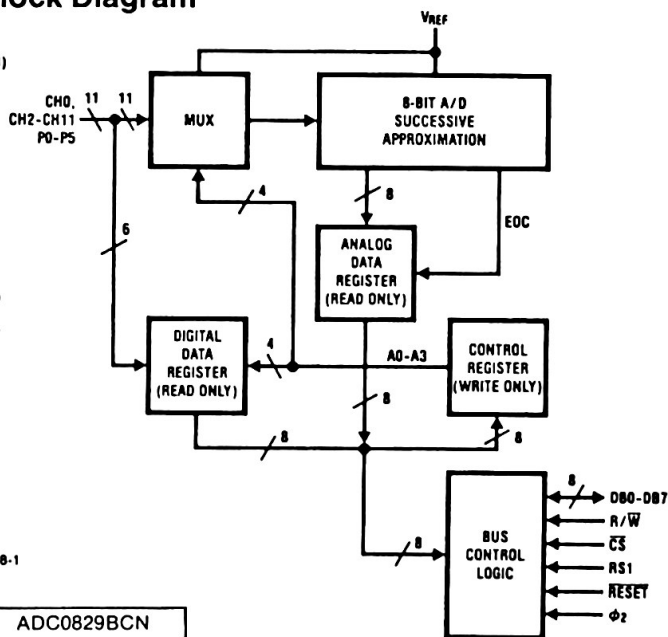
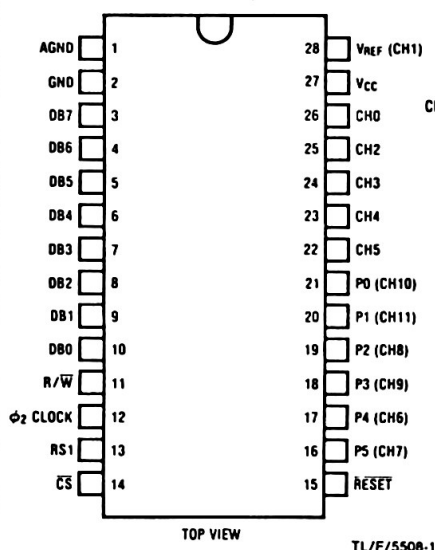
■ Resolution	8 Bits
■ Total Unadjusted Error	$\pm 1/2$ LSB and ± 1 LSB
■ Conversion Time	256 μ S
■ Single Supply	5V _{DC}
■ Low Power	50 mW

Features

- No missing codes
- Operates ratiometrically or with analog span adjusted voltage reference
- 11-Channel multiplexer with latched control logic of which six can be used as digital inputs
- Easy interface to all microprocessors or operates "stand alone"
- 0 to 5V analog input range with single 5V supply
- T2 L/MOS input/output compatible
- No zero or full scale adjusts required
- Standard 28-pin DIP
- Temperature range -40°C to $+85^{\circ}\text{C}$

Connection Diagram

Block Diagram



Ordering Information

Error	$\pm 1/2$ Bit Unadjusted	ADC0829BCN
	± 1 Bit Unadjusted	ADC0829CCN
Package Outline		N28B

ADC1001, ADC1021 10-Bit μ P Compatible A/D Converters

General Description

The ADC1001 and ADC1021 are CMOS, 10-bit successive approximation A/D converters. The 20-pin ADC1001 is pin compatible with the ADC0801 8-bit A/D family. The 10-bit data word is read in two 8-bit bytes, formatted left justified and high byte first. The six least significant bits of the second byte are set to zero, as is proper for a 16-bit word.

The 24-pin ADC1021 outputs 10 bits in parallel and is intended for interface to a 16-bit data bus.

A differential analog voltage input allows increasing the common-mode rejection and offsetting the analog zero input voltage value. In addition, the voltage reference input can be adjusted to allow encoding any smaller analog voltage span to the full 10 bits of resolution.

- Easily interfaced to 6800 μ P derivatives with minimal external logic
- Differential analog voltage inputs
- Logic inputs and outputs meet both MOS and T²L voltage level specifications
- Works with 2.5V (LM336) voltage reference
- On-chip clock generator
- 0V to 5V analog input voltage range with single 5V supply
- Operates ratiometrically or with 5 V_{DC}, 2.5 V_{DC}, or analog span adjusted voltage reference
- 0.3" standard width 20-pin DIP package or 24 pins with 10-bit parallel output

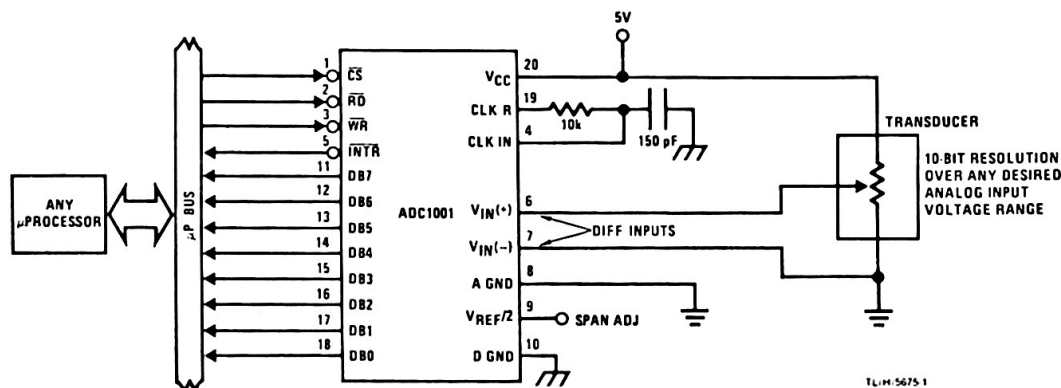
Features

- ADC1001 is pin compatible with ADC0801 series 8-bit A/D
- Compatible with NSC800 and 8080 μ P derivatives — no interfacing logic needed

Key Specifications

- | | |
|-------------------|-------------|
| ■ Resolution | 10 bits |
| ■ Linearity error | ± 1 LSB |
| ■ Conversion time | 200 μ s |

Typical Application



ADC1210, ADC1211 12-Bit CMOS A/D Converters

General Description

The ADC1210, ADC1211 are low power, medium speed, 12-bit successive approximation, analog-to-digital converters. The devices are complete converters requiring only the application of a reference voltage and a clock for operation. Included within the device are the successive approximation logic, CMOS analog switches, precision laser trimmed thin film R-2R ladder network and FET input comparator.

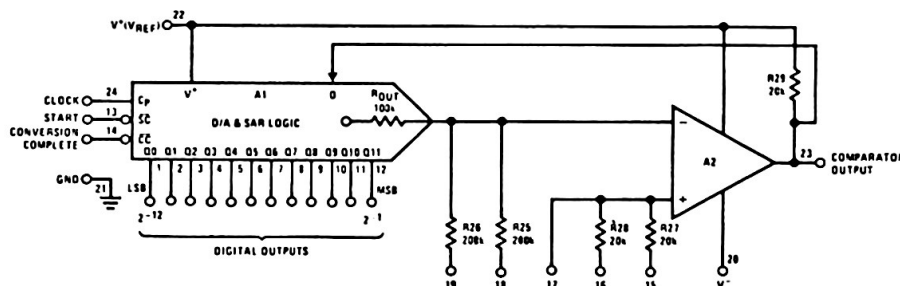
The ADC1210 offers 12-bit resolution and 12-bit accuracy, and the ADC1211 offers 12-bit resolution with 10-bit accuracy. The inverted binary outputs are directly compatible with CMOS logic. The ADC1210, ADC1211 will operate over a wide supply range, convert both bipolar and unipolar analog inputs, and operate in either a continuous conversion mode or logic-controlled START-STOP conversion mode. The devices are capable of making a 12-bit conversion in 100 μ s typ, and can be connected to convert 10 bits in 30 μ s.

Both devices are available in military and industrial temperature ranges.

Features

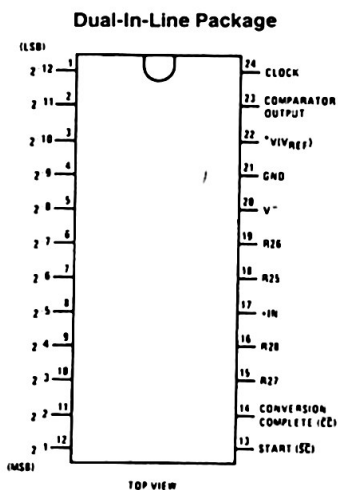
- 12-bit resolution
- $\pm 1/4$ LSB or ± 2 LSB nonlinearity
- Single +5V to ± 15 V supply range
- 100 μ s 12-bit, 30 μ s 10-bit conversion rate
- CMOS compatible outputs
- Bipolar or unipolar analog inputs
- 200 k Ω analog input impedance

Block Diagram



TL/H/5677-1

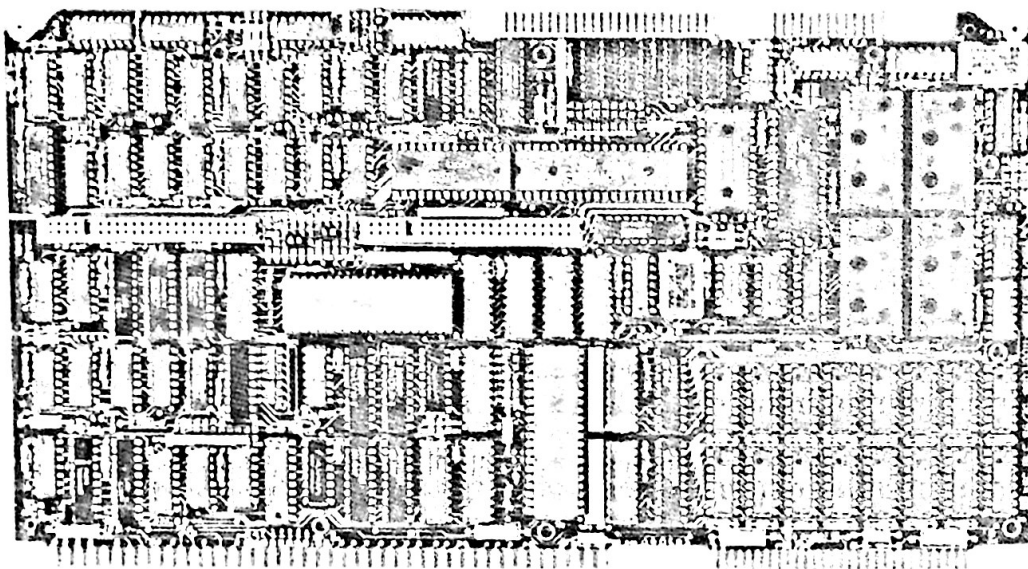
Connection Diagram



Order Number ADC1210HD,
ADC1210HCD, ADC1211HD,
ADC1211HCD
See NS Package D24D

TL/H/5677-2

BLC™-86/30 Board Level Computer



TL/T/5527-1

- 8086-2 Microprocessor based, 5 or 8 MHz operation
- 128K bytes of dual-port RAM, expandable on-board to 256KB
- Socked for up to 64K bytes of JEDEC standard 24/28 pin memory devices
- 24 programmable parallel I/O lines
- Programmable synchronous/asynchronous RS232 serial interface
- Two programmable 16-bit BCD or binary timers
- 9 levels of vectored interrupts
- Fully Multibus compatible
- Optional BLX™-337, 8087 co-processor module
- Two BLX bus expansion connectors

Product Overview

The BLC-86/30 is a high performance 8086-2 based CPU board with up to a quarter megabyte of on-board, dual port RAM and 64KB of PROM space. It provides optimum performance by not having to utilize the bus for most memory operations and in certain applications, provides a single board solution. This allows for true parallel processing in multimaster systems.

The BLC-86/30 can operate at 5 MHz, in order to maintain full software compatibility with the 86/12 CPU board or to accommodate the BLC-337, 8087 based co-processor module. It can also operate at 8 MHz.

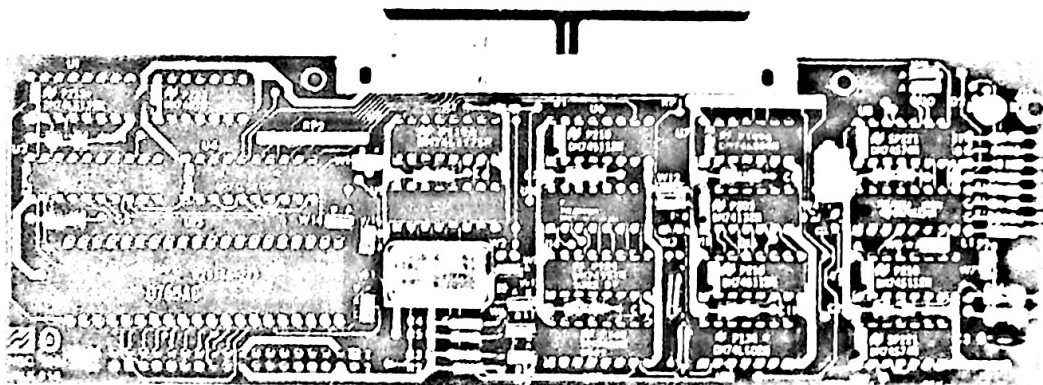
Functional Description

Central Processor Unit

The CPU for the BLC-86/30 board is the 8086-2 microprocessor and is jumper selectable to operate at either 5 or 8 MHz. The 8086-2 is partitioned logically into two processing units; the Bus Interface Unit (BIU) and the Execution Unit (EU). These two units perform as separate asynchronous operational processors. The BIU provides basic bus control as well as functions related to instruction fetching and queuing, operand fetch and store and address location. Up to 6 bytes of the instruction stream can be queued while

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BLX™-218 FLOPPY DISK CONTROLLER



TL/T/5509-3

- Controls up to 4 drives with 8 surfaces
- Controls either 8" or 5.25" drives
- Supports either single or double density formats
- Fully BLX compatible
- Single +5V requirement
- On-board phase locked loop

Product Overview

The BLX-218 floppy disk controller is a new member of National's Series/80 family of Multibus products. The BLX-218 is fully compatible with any board utilizing the BLX on-board I/O expansion interface. This product provides an easy to use, high performance mass storage interface. Numerous user selectable options are designed in making it easy to use in a wide variety of applications.

Functional Description

The BLX-218 floppy disk controller is capable of supporting virtually any 8" or 5.25" drive and can man-

age up to four drives with a maximum of eight surfaces. The BLX-218 will support the IBM 3740 single density, IBM System 34 double density or other formats with sector lengths up to 8192 bytes. The individual drive operating characteristics are specified under program control.

The BLX-218 can also perform operations in either single or multiple sectors and has on-board data separation logic which performs data encoding and decoding. In addition, this module can operate in either a DMA or non DMA environment.

DAC1265A, DAC1265 Hi-Speed 12-Bit D/A Converter with Reference

General Description

The DAC1265A and DAC1265 are fast 12-bit digital to analog converters with internal voltage reference. These DACs use 12 precision high speed bipolar current steering switches, control amplifier, thin film resistor network, and buried zener voltage reference to obtain a high accuracy, very fast analog output current. The DAC1265A and DAC1265 have 10%–90% full-scale transition time under 35 ns and settle to less than $\frac{1}{2}$ LSB in 200 ns. The buried zener reference has long-term stability and temperature drift characteristics comparable to the best discrete or separate IC references.

These digital to analog converters are recommended for applications in CRT displays, precision instruments and data acquisition systems requiring throughput rates as high as 5 MHz for full range transitions.

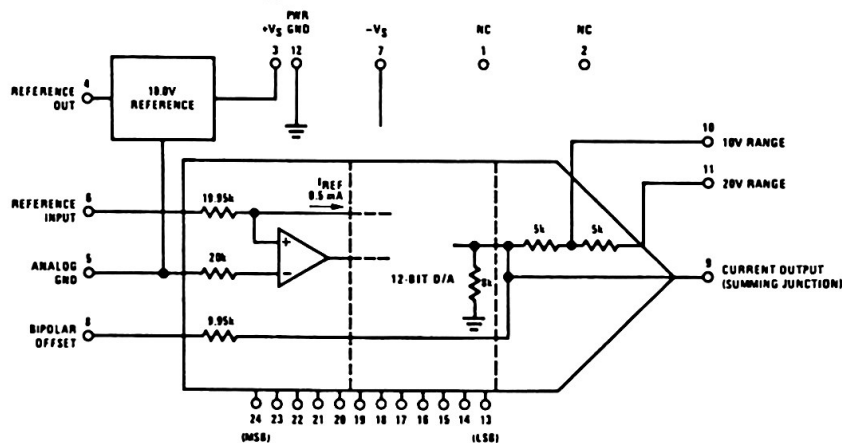
Features

- Bipolar current output DAC and voltage reference
- Fully differential, non-saturating precision current switch — R_{OUT} and C_{OUT} do not change with digital input code
- Internal buried zener reference — $10V \pm 1\%$ max
- Precision thin film resistors for use with external op amp for voltage out or as input resistors for a successive approximation A/D converter
- Superior replacement for 12-bit D/A converters of this type

Key Specifications

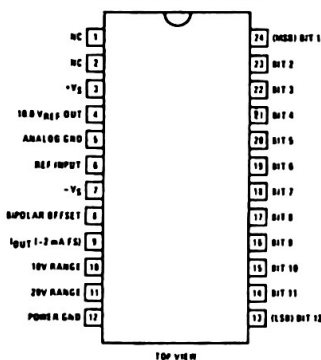
- Resolution and Monotonicity 12 Bits
- Linearity 12 Bits
(Guaranteed over temperature)
- Output Current Settling Time 400 ns max to 0.01%
- Gain Tempco ± 15 ppm/ $^{\circ}C$ max
- Power Supply Sensitivity ± 10 ppm of FS/% V_{SUPPLY}

Block and Connection Diagrams



TL/H/5242-1

Dual-In-Line Package



TOP VIEW

TL/H/5242-2

DH0011A High Voltage High Current Driver

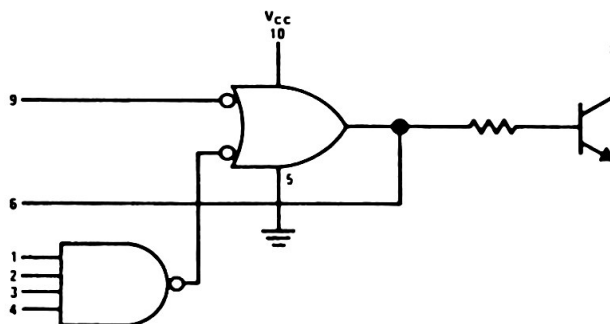
General Description

The DH0011A High Voltage, High Current Driver family consists of hybrid integrated circuits which provide a wide range of variations in temperature range, package, and output current drive capability.

Applications include driving lamps, relays, cores, and

other devices requiring several hundred milliamp currents at voltages up to 50V. Logic flexibility is provided through a 4-input NAND gate, a NOR input and an input which bypasses the gating and connects to the base of the output transistor.

Logic Diagram



TL/K/6863-1

Ordering Information

NSC Designation	Package	Temperature Range	Output Capability
DH0011AH	H10C	-55°C to +125°C	500mA

DM77/87SR27, DM77/87SR27B (512 × 8) 4K-Bit Registered TTL PROM

General Description

The DM77/87SR27 is an electrically programmable Schottky TTL read-only memory with D-type, master-slave registers on-chip. This device is organized as 512 words by 8 bits and is available in the TRI-STATE[®] output version. Designed to optimize system performance, this device also substantially reduces the cost and size of pipelined micro-programmed systems and other designs wherein accessed PROM data is temporarily stored in a register. The DM77/87SR27 also offers maximal flexibility for memory expansion and data bus control by providing both synchronous and asynchronous output enables. All outputs will go into the "OFF" state if the synchronous chip enable (\overline{GS}) is high before the rising edge of the clock, or if the asynchronous chip enable (\overline{G}) is held high. The outputs are enabled when \overline{GS} is brought low before the rising edge of the clock and \overline{G} is held low. The \overline{GS} flip-flop is designed to power up to the "OFF" state with the application of V_{CC} .

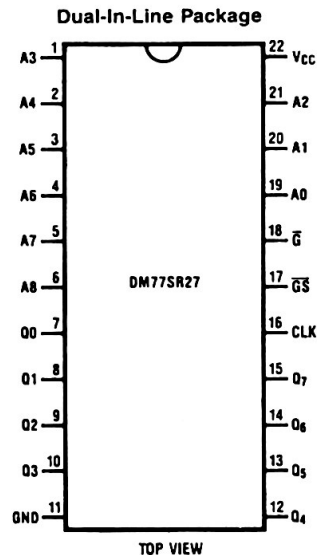
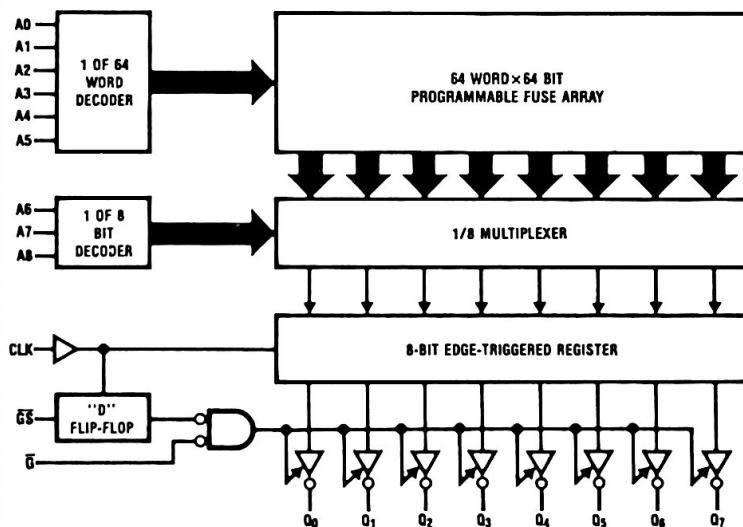
Data is read from the PROM by first applying an address to inputs A0-A8. During the setup time the output of the array is loaded into the master flip-flop of the data register. During the rising edge (low to high transition) of the clock, the data is then transferred to the slave of the flip-flop and will appear on the output if the output is enabled. Following the rising edge clock transition the addresses and synchronous chip enable can be removed and the output data will remain stable.

PROMs are shipped from the factory with lows in all locations. A high may be programmed into any selected location by following the programming instructions. Once programmed, it is impossible to go back to a low.

Features

- Functionally compatible with Am27S27
- On-chip, edge-triggered registers
- Synchronous and asynchronous enables for word expansion
- 22-pin 400-mil thin-DIP package
- 35 ns address setup and 20 ns clock to output for maximum system speed
- Highly reliable, titanium tungsten fuses
- TRI-STATE outputs
- Low voltage TRI-SAFE[™] programming
- All parameters guaranteed over temperature

Block and Connection Diagrams



TUL6686-1

TUL6686-2

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DS8910 AM-Only Digital Phase-Locked Loop Frequency Synthesizer

General Description

The DS8910 is a PLL synthesizer designed specifically for use in AM radios. It contains the reference oscillator, a phase comparator, a charge pump, an operational amplifier, a 15 MHz ECL/I²L dual modulus programmable divider, and a 19-bit shift register/latch for serial data entry. The device is designed to operate with a serial data controller generating the necessary division codes for each frequency, and logic state information for radio function inputs/outputs.

A 3.96 MHz pierce oscillator and divider chain generate a 1.98 MHz external controller clock, a 20 kHz, 10 kHz, 9 kHz, and 1 kHz reference signals, and a 50 Hz time-of-day signal. The oscillator and divider chain are sourced by the V_{CCM} pin thus providing a low power controller clock drive and time-of-day indication when the balance of the PLL is powered down.

The 21-bit serial data stream is transferred between the frequency synthesizer and the controller via a 3-wire bus system comprised of a data line, a clock line, and an enable line.

The first 2 bits in the serial data stream address the synthesizer thus permitting other devices such as display drivers to share the same bus. The next 14 bits are used for the PLL (N + 1) divide code. The 15th bit is a "don't care" bit and serves no function. The 16th and 17th bits are used to select one of the 4 reference frequencies. The 18th and 19th bits are connected via latches to open collector outputs. These outputs can be used to drive radio functions such as gain, mute, AM, or charge pump current source levels.

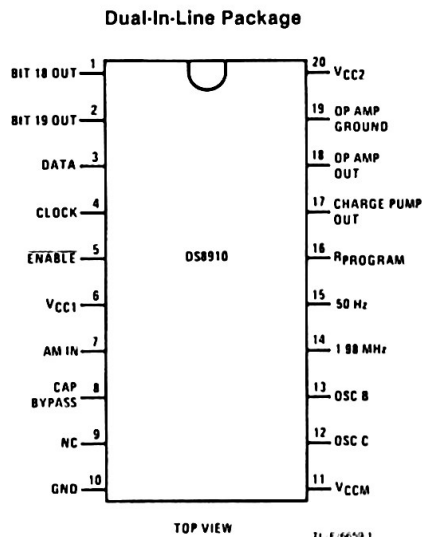
The PLL consists of a 14-bit programmable I²L divider, an ECL phase comparator, an ECL dual modulus (p/p + 1) prescaler, a high speed charge pump, and an operational amplifier. The programmable divider divides by (N + 1), N being the number loaded into the shift register. The programmable divider is clocked through a $\div 7/8$ prescaler by the AM input. The AM input will work at frequencies up to 15 MHz. The VCO can be tuned with a frequency resolution of either 1 kHz, 9 kHz, 10 kHz, or 20 kHz. The buffered AM input is self-biased and can be driven directly by the VCO through a capacitor. The ECL phase comparator produces very accurate resolution of the phase difference between the input signal and the reference oscillator. The high speed charge pump consists of a switchable constant current source and sink. The charge pump can be programmed to deliver from 75 μ A to 750 μ A of constant current by connection of an external resistor from pin R_{PROGRAM} to ground or the open collector bit outputs. Connection of programming resistors to the bit outputs enables the controller to adjust the loop gain for the particular reference frequency selected. The charge pump will source current if the VCO frequency is high and sink current if the VCO frequency is low. The low noise operational amplifier pro-

vided has a high impedance JFET input and a large output voltage range. The op amp's negative input is common with the charge pump output and its positive input is internally biased.

Features

- Uses inexpensive 3.96 MHz reference crystal
- Serial data entry for simplified control
- 50 Hz output for time-of-day reference driven from separate low power V_{CCM}
- 2 open collector buffered outputs for controlling various radio functions or loop gain
- AM input has 15 mV (typical) hysteresis
- Programmable charge pump current sources enable adjustment of system loop gain
- Operational amplifier provides high impedance load to charge pump output and a wide voltage range for the VCO input

Connection Diagram



ECL Programmable Array Logic (PAL®) Family

General Description

The PL1016P8/10016P8 is the first member of an ECL programmable logic device family possessing common electrical characteristics, utilizing an easily accommodated programming procedure, and produced with National Semiconductor's advanced oxide-isolated process. This family includes both latched and registered output devices.

These devices are fabricated using National's proven Ti-W (Titanium-Tungsten) fuse technology to allow fast, efficient, and reliable programming.

This family allows the designer to quickly implement the defined logic function by removing the fuses required to properly configure the internal gates and/or registers. Product terms with all fuses removed assume a logical high state. All devices in this series are provided with an output polarity fuse that, if removed, will permit any output to independently provide a logic low when the equation is satisfied. When these fuses are intact the outputs provide a logic true (most positive voltage level) in response to the input conditions defined by the applicable equation.

The registers, in selected devices, consist of D-type flip-flops which are loaded in response to the low-to-high transition of the clock. Fuse symbols have been omitted from the logic diagrams to allow the designer use of the diagrams to create fuse maps representing the programmed device.

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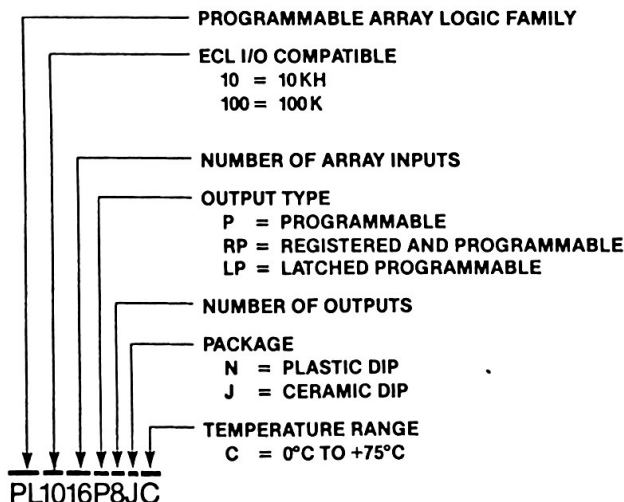
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All devices in this family can be programmed using conventional programmers. After the device has been programmed and verified, an additional fuse may be removed to inhibit further verification or programming. This "security" feature can provide a proprietary circuit which cannot easily be duplicated.

Features

- Programmable replacement for conventional ECL logic.
- Offered in a 10KH I/O compatible version with a 100K version coming.
- Simplifies prototyping and board layout.
- 24-pin thin DIP packages.
(0.300-10KH version, 0.400-100K version)
- Programmed on standard PAL programmers.
- Special feature reduces possibility of copying by competitors.
- Reliable titanium-tungsten fuses.

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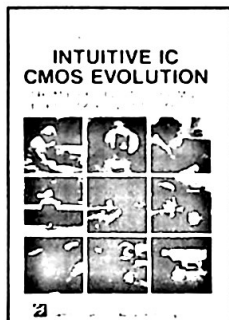
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LMC835 Digital Controlled Graphic Equalizer

General Description

The LMC835 is a monolithic, digitally-controlled graphic equalizer CMOS LSI for Hi-Fi audio. The LMC835 consists of a Logic section and a Signal Path section made of analog switches and thin-film silicon-chromium resistor networks. The LMC835 is used with external resonator circuits to make a stereo equalizer with seven bands, ± 12 dB or ± 6 dB gain range and 25 steps each. Only three digital inputs are needed to control the equalization. The LMC835 makes it easy to build a μ P-controlled equalizer.

The signal path is designed for very low noise and distortion, resulting in very high performance, compatible with PCM audio.

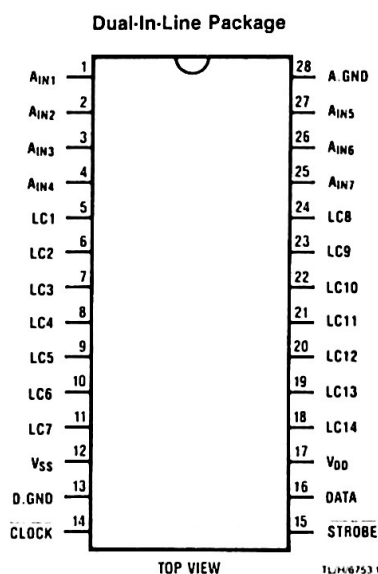
Features

- No volume controls required
- Three-wire interface
- 14 bands, 25 steps each
- ± 12 dB or ± 6 dB gain ranges
- Low noise and distortion
- TTL, CMOS logic compatible

Applications

- Hi-Fi equalizer
- Receiver
- Car stereo
- Musical instrument
- Tape equalization
- Mixer
- Volume controller

Connection Diagram



LH0132/LH0132C

Ultra-Fast FET-Input Operational Amplifier

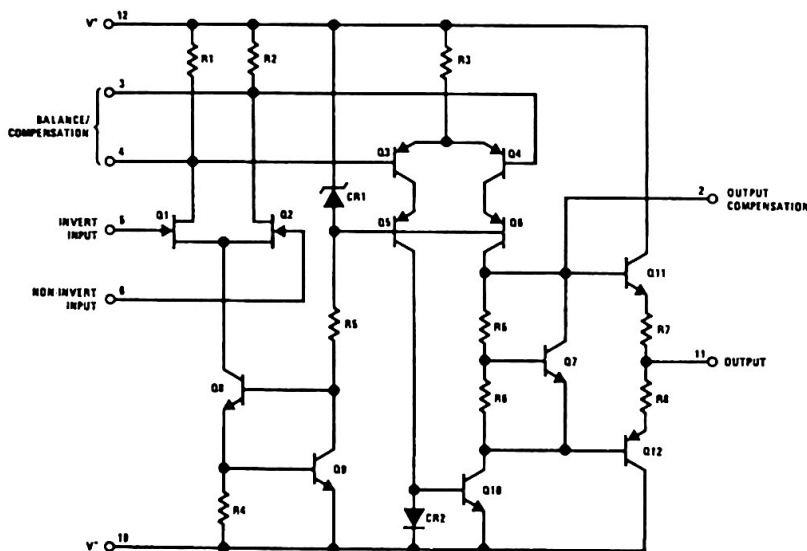
General Description

The LH0132 is a high slew rate, high input impedance differential amplifier. It was developed specifically for sample and hold and other fast signal handling applications which require very low input currents over the full input voltage range. Input offset and bias currents are guaranteed over a full input common mode range of -10 volts to $+10$ volts.

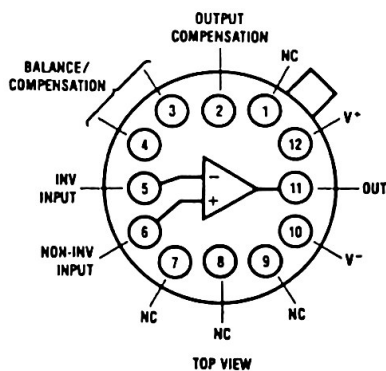
Features

- 100 pA I_{bias} at $V_{\text{IN}} = \pm 8\text{V}$
- $500 \text{ V}/\mu\text{s}$ slew rate
- 70 MHz bandwidth
- 5 mV offset voltage
- FET input
- No compensation for gains above 50
- Peak output current to 100 mA

Block and Connection Diagrams



TL/K/5499-4



TL/K/5499-5

LM133/LM333/LM333A 3-Ampere Adjustable Negative Regulators

General Description

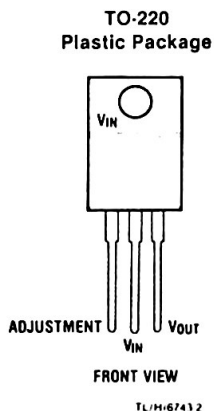
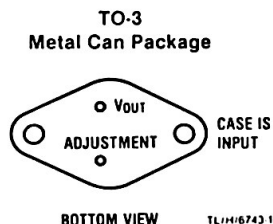
The LM133/LM333/LM333A are adjustable 3-terminal negative voltage regulators capable of supplying in excess of -3.0A over an output voltage range of -1.2V to -32V . These regulators are exceptionally easy to apply, requiring only 2 external resistors to set the output voltage and 1 output capacitor for frequency compensation. The circuit design has been optimized for excellent regulation and low thermal transients. Further, the LM133 series features internal current limiting, thermal shutdown and safe-area compensation, making them virtually blowout-proof against overloads.

The LM133/LM333/LM333A serve a wide variety of applications including local on-card regulation, programmable-output voltage regulation or precision current regulation. The LM133/LM333/LM333A are ideal complements to the LM150/LM250/LM350 adjustable positive regulators.

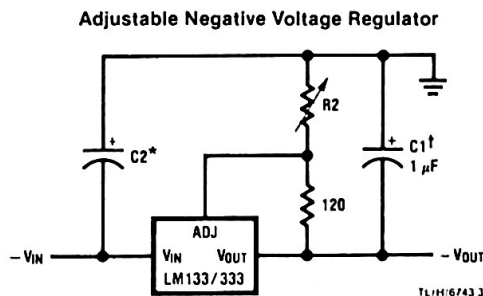
Features

- Output voltage adjustable from -1.2V to -32V
- 3.0A output current guaranteed, -55°C to $+150^\circ\text{C}$
- Line regulation typically $0.01\%/V$
- Load regulation typically 0.1%
- Excellent rejection of thermal transients
- $50\text{ ppm}/^\circ\text{C}$ temperature coefficient
- Temperature-independent current limit
- Internal thermal overload protection
- 100% electrical burn-in
- Standard 3-lead transistor package

Connection Diagrams



Typical Applications



$$-V_{OUT} = -1.25V \left(1 + \frac{R_2}{120\Omega} \right) + (-I_{ADJ} \times R_2)$$

$C_1 = 1\text{ }\mu\text{F}$ solid tantalum or $10\text{ }\mu\text{F}$ aluminum electrolytic required for stability.

* $C_2 = 1\text{ }\mu\text{F}$ solid tantalum is required only if regulator is more than $4''$ from power supply filter capacitor.

Output capacitors in the range of $1\text{ }\mu\text{F}$ to $1000\text{ }\mu\text{F}$ of aluminum or tantalum electrolytic are commonly used to provide improved output impedance and rejection of transients.

LM592/LM592A Differential Video Amp

General Description

The LM592 is a two stage differential input, differential output, wideband video amplifier. The use of internal series-shunt feedback gives wide bandwidth with low phase distortion and high gain stability. Emitter follower outputs provide low output impedances necessary to drive capacitive loads. This device offers fixed gains of 100 and 400 with no external components plus the flexibility of adjusting the gain from 0 to 400 with the addition of a single resistor. This flexibility also allows the device to be configured as a high pass, low pass, or band pass filter.

The LM592 is ideal for use in magnetic memory systems. The device is also very useful as a video and pulse amplifier in video recorders and other communications systems.

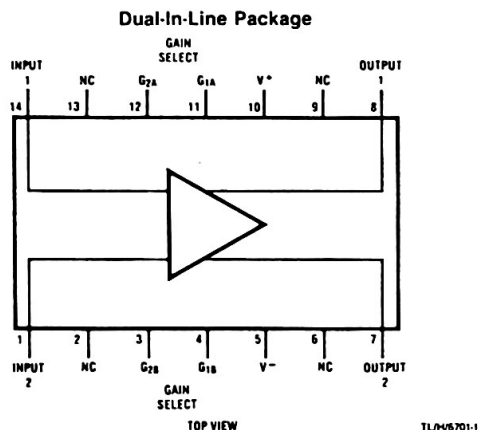
Features

- 120 Mhz bandwidth
- Adjustable gains from 0 to 400
- Adjustable pass band
- No frequency compensation required

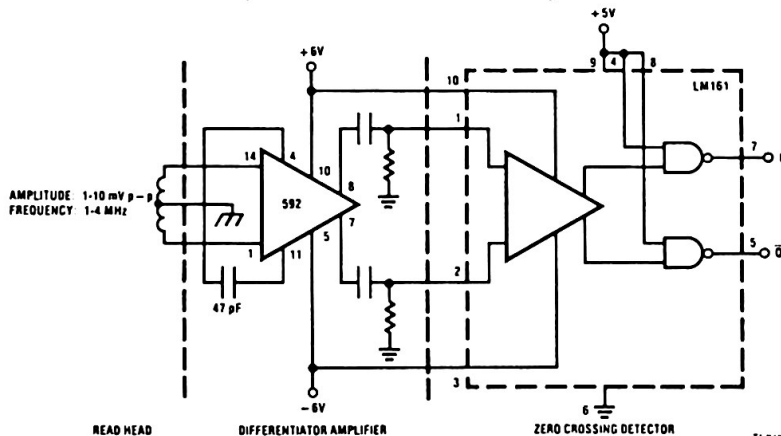
Applications

- Disc file memories
- Magnetic tape systems
- Thin film or plated wire memories
- Wide band video amplifiers

Connection Diagram



Disc/Tape Phase Modulated Readback Systems



LM832 Dynamic Noise Reduction System DNR™

General Description

The LM832 is a stereo noise reduction circuit for use with audio playback systems. The DNR system is noncomplementary, meaning it does not require encoded source material. The system is compatible with virtually all prerecorded tapes and FM broadcasts. Psychoacoustic masking, and an adaptive bandwidth scheme allow the DNR to achieve 10 dB of noise reduction. DNR can save circuit board space and cost because of the few additional components required.

The LM832 is optimized for low voltage operation with input levels around 30 mVrms.

For higher input levels use the LM1894.

DNR™ is a trademark of National Semiconductor Corp.
 The DNR™ system is licensed to National Semiconductor Corp. under U.S. patent 3,678,416 and 3,753,159.
 Contact National Semiconductor for use of DNR™ logo.
 A trademark and licensing agreement is required for the use of this product.

Features

- Low voltage battery operation
- Non-complementary noise reduction, "single ended"
- Low cost external components, no critical matching
- Compatible with all prerecorded tapes and FM
- 10 dB effective tape noise reduction CCIR/ARM weighted
- Wide supply range, 1.5V to 9V
- 150 mVrms input overload
- No royalty requirements
- Cascade connection for 17 dB noise reduction

Applications

- Headphone stereo
- Microcassette players
- Radio cassette players
- Automotive radio/tape players

Application Circuit

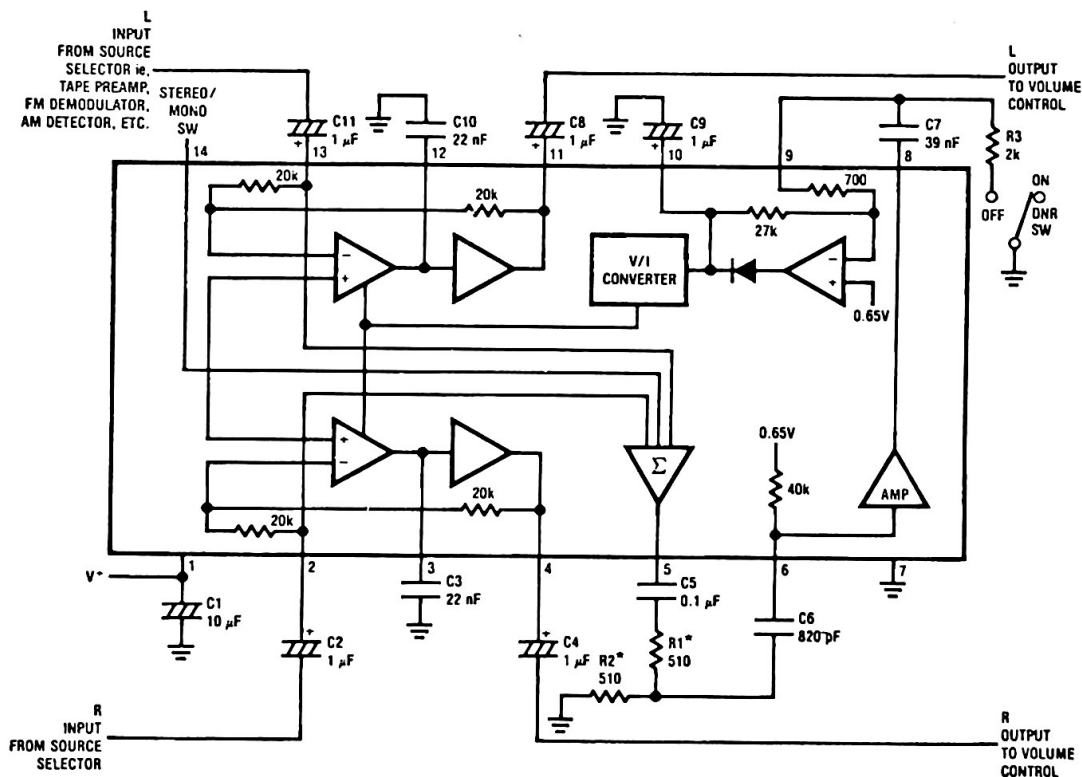


FIGURE 1. Component Hook-up for Stereo DNR System

TL/H/5178-1

LM833 Dual Audio Operational Amplifier

General Description

The LM833 and LM833A are dual general purpose operational amplifiers designed with particular emphasis on performance in audio systems.

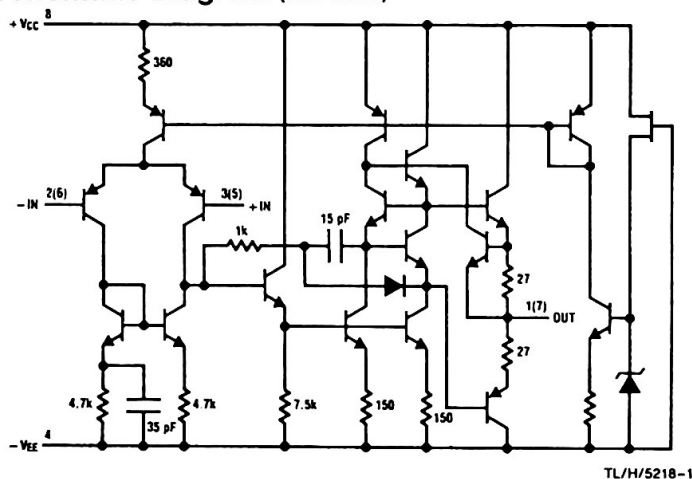
These dual amplifier ICs utilize new circuit and processing techniques to deliver low noise, high speed and wide bandwidth without increasing external components or decreasing stability. The LM833 and LM833A are internally compensated for all closed loop gains and are therefore optimized for all preamp and high level stages in PCM and HiFi systems. The LM833 and LM833A are pin for pin compatible with industry standard dual operational amplifiers.

The LM833A guarantees low noise for noise critical applications by 100% noise testing.

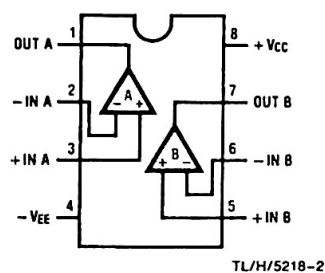
Features

- Wide dynamic range > 140 dB
- Low input noise voltage $4.5 \text{ nV}/\sqrt{\text{Hz}}$
- High slew rate $7 \text{ V}/\mu\text{s}$ (typ)
 $5 \text{ V}/\mu\text{s}$ (min)
- High gain bandwidth product 15 MHz (typ)
 10 MHz (min)
- Wide power bandwidth 120 kHz
- Low distortion 0.002%
- Low offset voltage 0.3 mV
- Large phase margin 60°

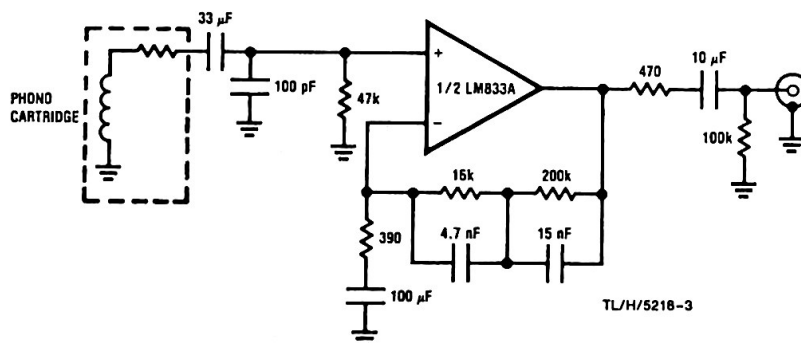
Schematic Diagram (1/2 LM833)



Connection Diagram



Typical Application RIAA Preamp



$A_v = 35 \text{ dB}$
 $E_n = 0.33 \mu\text{V}$
 $S/N = 90 \text{ dB}$
 $f = 1 \text{ kHz}$
 A Weighted
 A Weighted, $V_{IN} = 10 \text{ mV}$
 $\phi f = 1 \text{ kHz}$

LM1014 Motor Speed Regulator

General Description

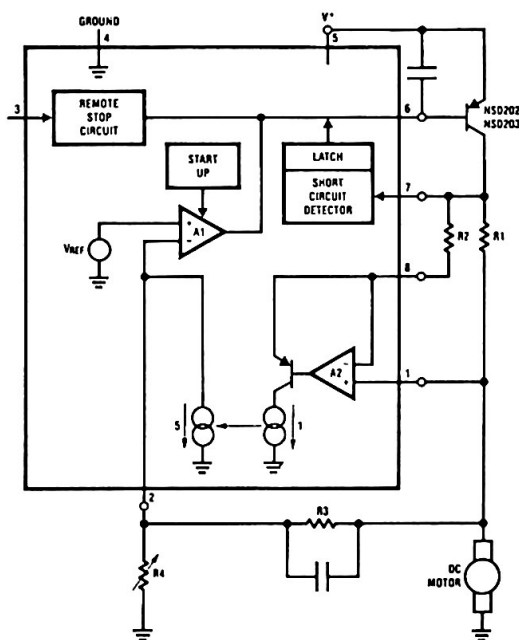
The LM1014 is a monolithic integrated circuit specifically designed to provide a low cost motor speed regulator for low voltage DC motors.

Features

- 5V to 20V operating voltage range
- Short circuit protection

- Remote pause control
- Saturation voltage 0.1V
- Motor connected to ground for ease of RF suppression
- Motor torque compensation
- Low current consumption

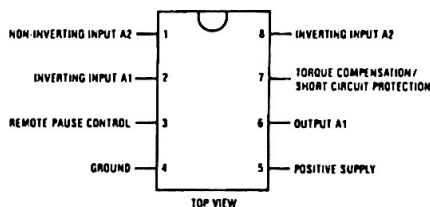
Functional Block Diagram



TL/H/6159-1

Connection Diagram

Dual-In-Line Package



TL/H/6159-2

LM1837 Low Noise Preamplifier for Autoreversing Tape Playback Systems

General Description

The LM1837 is a dual autoreversing high gain tape preamplifier for applications requiring optimum noise performance. It has forward (left, right) and reverse (left, right) inputs which are selectable through a high impedance logic pin. It is an ideal choice for a tape playback amplifier when a combination of low noise, autoreversing, good power supply rejection, and no power-up transients are desired. The application also provides transient-free muting with a single pole grounding switch.

Features

- Programmable turn-on delay
- Transient-free power-up - no pops
- Transient-free muting
- Low noise - $0.6 \mu\text{V}$ CCIR/ARM in a DIN circuit referenced to gain at 1 kHz
- Low voltage battery operation - 4V
- Wide gain bandwidth due to broadband two amplifier approach - 76 dB @ 20 kHz
- High power supply rejection - 95 dB
- Low distortion - 0.03%
- Fast slew rate - $6\text{V}/\mu\text{s}$
- Short circuit protection
- Internal diodes for diode switching applications
- Low cost external parts
- Excellent low frequency response
- Prevents "click" from being recorded onto the tape during power supply cycling in tape playback applications
- High impedance logic pin for forward/reverse switching

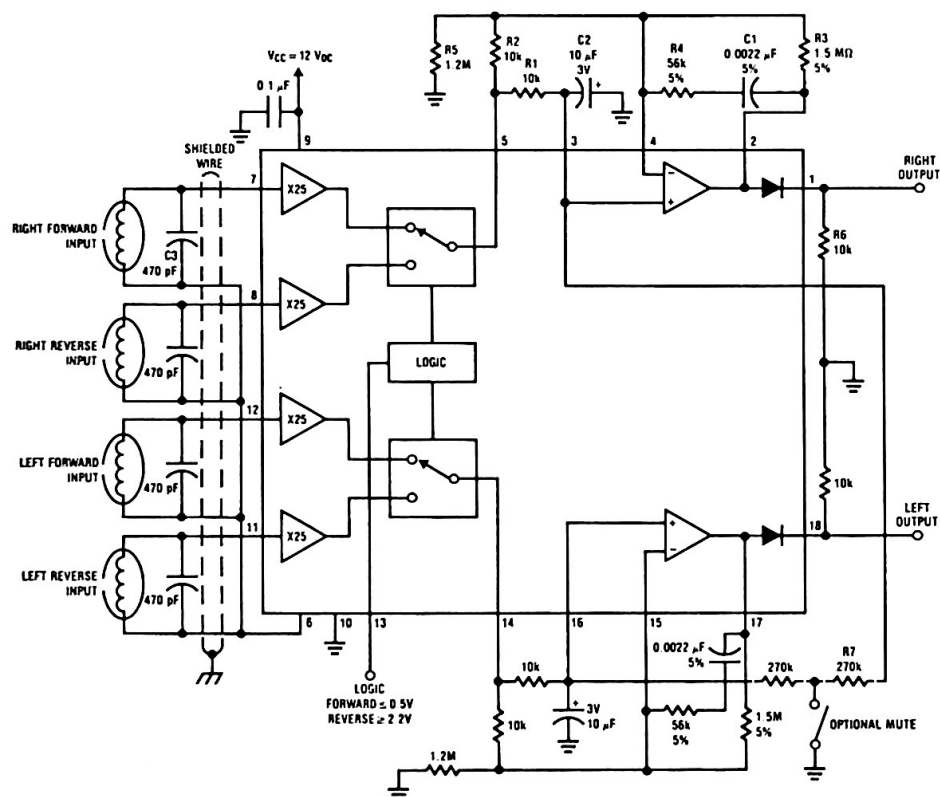


FIGURE 1. Autoreversing Tape Playback Application

TL/M/7902 1

LM2889 TV Video Modulator

General Description

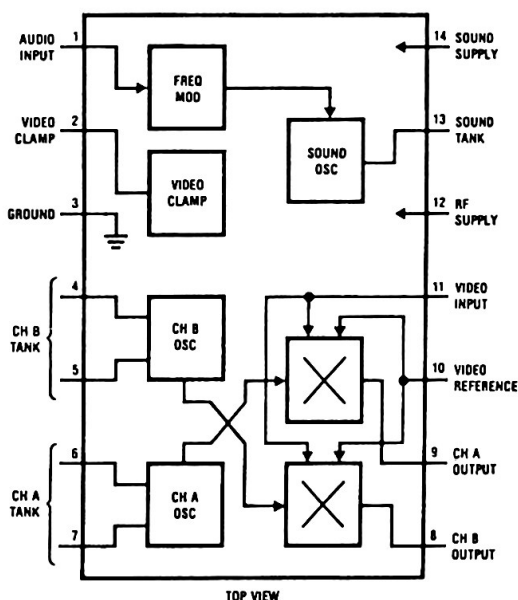
The LM2889 is designed to interface audio and video signals to the antenna terminals of a TV receiver. It consists of a sound subcarrier oscillator and FM modulator, video clamp, and RF oscillators and modulators for two low-VHF channels.

The LM2889 allows video information from VTRs, video disk systems, games, test equipment, or similar sources to be displayed on black and white or color TV receivers.

Features

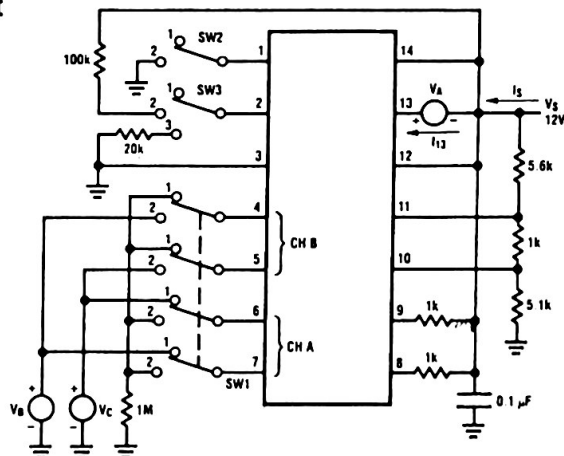
- Pin for pin compatible with LM1889 RF section
- Low distortion FM sound modulator (less than 1% THD)
- Video clamp for AC-coupled video
- Low sound oscillator harmonic levels
- 10V to 16V supply operation
- DC channel switching
- Excellent oscillator stability
- Low intermodulation products

Block and Connection Diagrams (Dual-In-Line Package)



Order Number LM2889N
See NS Package Number N14A

DC Test Circuit



TL/H/5079-1

LM3361A Low Voltage/Power Narrow Band FM IF System

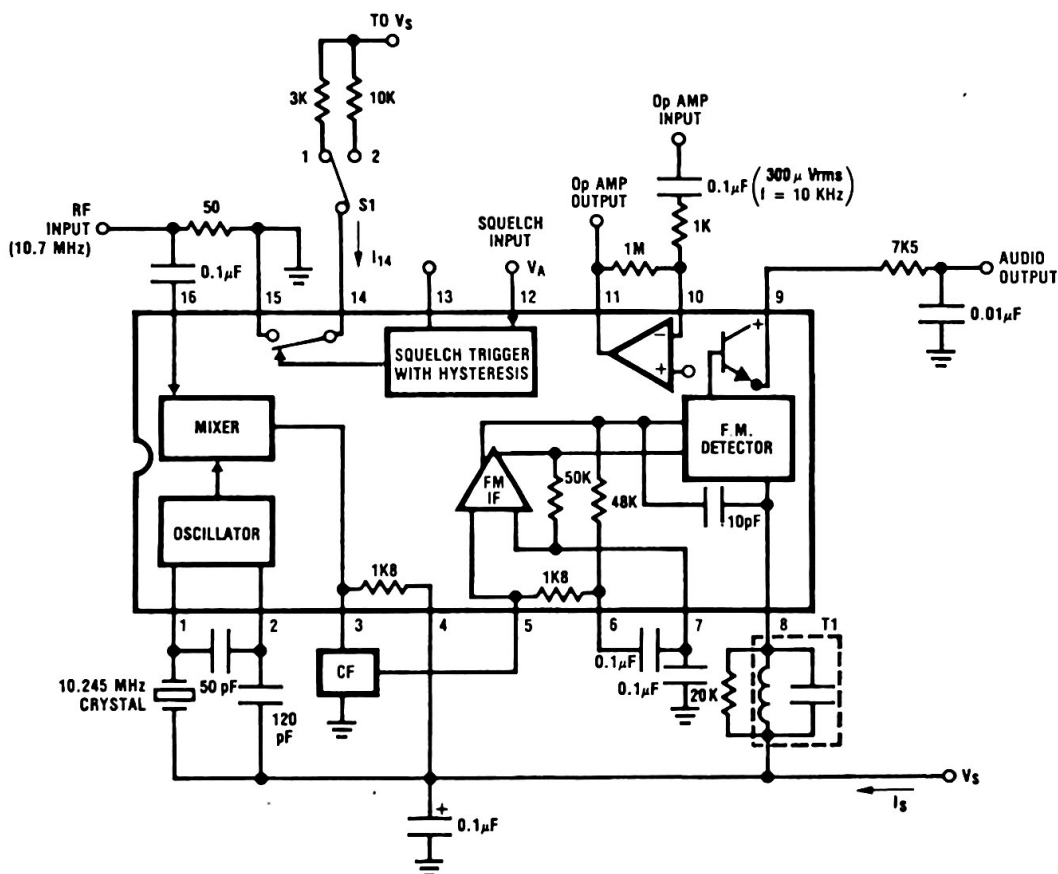
General Description

The LM3361A contains a complete narrow band FM demodulation system operable to less than 2V supply voltage. Blocks within the device include an oscillator, mixer, FM IF limiting amplifier, FM demodulator, op amp, scan control, and mute switch. The LM3361A is similar to the MC3361 with the following improvements: the LM3361A has higher voltage swing both at the op amp and audio outputs. It also has lower nominal drain current and a squelch circuit that draws significantly less current than the MC3361. Device pinout functions are identical with some slightly different operating characteristics.

Features

- Functions at low supply voltage (less than 2V)
- Highly sensitive (-3 dB limiting at $2.0 \mu\text{V}$ input typical)
- High audio output (increased 6 dB over MC3361)
- Low drain current (2.8 mA typ. , $V_{CC} = 3.6\text{V}$)
- Minimal drain current increase when squelched
- Low external parts count

Block Diagram And Test Circuit



T1-TOKO RMC-2A6597HM
CF-MURATA CFU 455E

TL/H/5586-1

LP339 Ultra-Low Power Quad Comparator

General Description

The LP339 consists of four independent voltage comparators designed specifically to operate from a single power supply and draw typically 60 μ A of power supply drain current over a wide range of power supply voltages. Operation from split supplies is also possible and the ultra-low power supply drain current is independent of the power supply voltage. These comparators also feature a common-mode range which includes ground, even when operated from a single supply.

Applications include limit comparators, simple analog-to-digital converters, pulse, square and time delay generators; VCO's; multivibrators; high voltage logic gates. The LP339 was specifically designed to interface with the CMOS logic family. The ultra-low supply current makes the LP339 valuable in battery powered applications.

Advantages

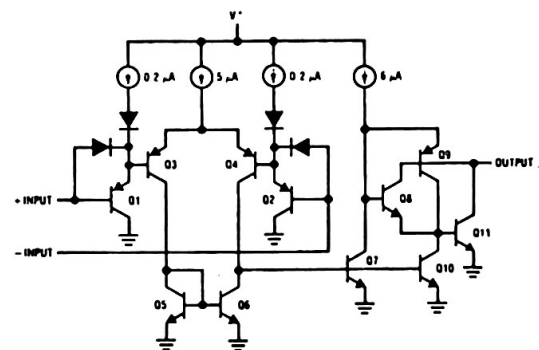
- Ultra-low power supply drain suitable for battery applications

- Single supply operation
- Sensing at ground
- Compatible with CMOS logic family
- Pin-out identical to LM339

Features

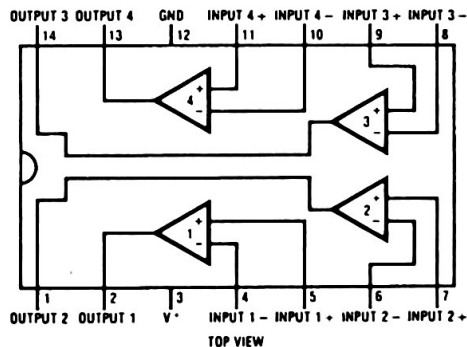
- Ultra-low power supply current drain (60 μ A) — independent of the supply voltage (75 μ W/comparator at +5 V_{DC})
- Low input biasing current 3 nA
- Low input offset current ± 0.5 nA
- Low input offset voltage ± 2 mV
- Input common-mode voltage includes ground
- Output voltage compatible with MOS and CMOS logic
- High output sink current capability (30 mA at V_O = 2 V_{DC})
- Supply Input protected against reverse voltages

Schematic and Connection Diagrams



TL/H/5226-1

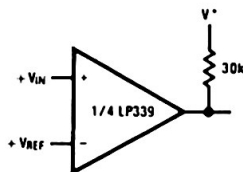
Dual-In-Line Package



TL/H/5226-2

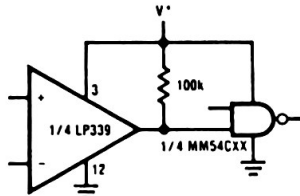
Typical Applications (V⁺ = 5.0 V_{DC})

Basic Comparator



TL/H/5226-3

Driving CMOS



TL/H/5226-4

MM58146/MM9016 TV Clock and Channel Display

General Description

The MM58146 and MM9016 TV Clock and Channel Display Circuit is a monolithic NMOS integrated circuit which generates a display of time and channel number on a television screen.

The chip contains a time of day clock and all the logic required to display time and a 2 digit channel number from an external source, such as the MM58142 TV Digital Tuning Chip.

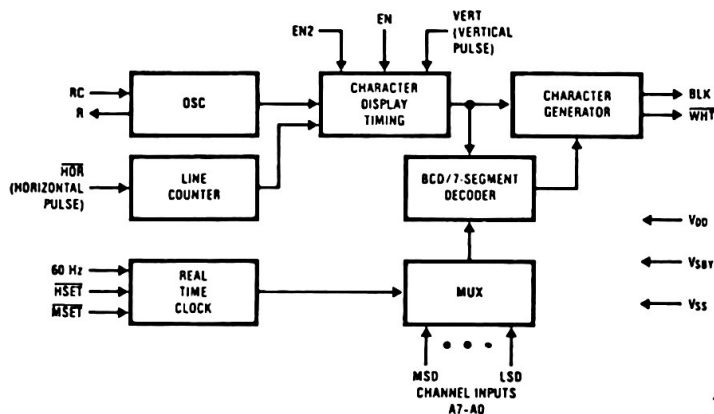
The horizontal, vertical and 60 Hz inputs and display outputs are designed to directly interface to the video system of many TV sets.

The time and channel number are displayed on the same line near the bottom of the screen.

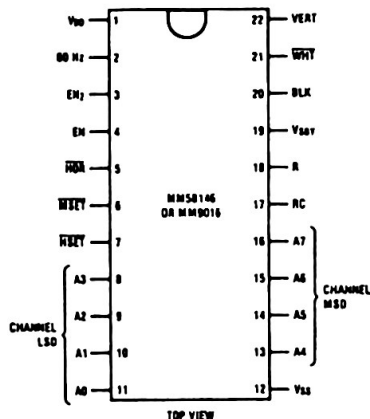
Features

- 12 hour operation
- Leading zero blanking on hours display
- Black border around white character
- Interfaces to video system directly on many TVs
- Clock and channel display or channel only display
- Two digit display need not be channel number. Channel number is entered as BCD

Block and Connection Diagrams



Dual-In-Line Package



MM58241 High Voltage Display Driver

General Description

The MM58241 is a monolithic MOS integrated circuit utilizing CMOS metal gate low threshold P and N-channel devices. It is available both in 40-pin molded dual-in-line packages or as dice. The MM58241 is particularly suited for driving high voltage (60V max) vacuum fluorescent (VF) displays (e.g., a 32-digit alphanumeric or dot matrix display).

Applications

- COPSTM or microprocessor-driven displays
- Instrumentation readouts
- Industrial control indicator
- Digital clock, thermostat, counter, voltmeter
- Word processor text displays
- Automotive dashboards

Features

- Direct interface to high voltage display
- Serial data input
- No external resistors required
- Wide display power supply operation
- LSTTL compatible inputs
- Software compatible with NS display driver family
- Compatible with alphanumeric or dot matrix displays
- Display blanking control input
- Simple to cascade

Block and Connection Diagrams

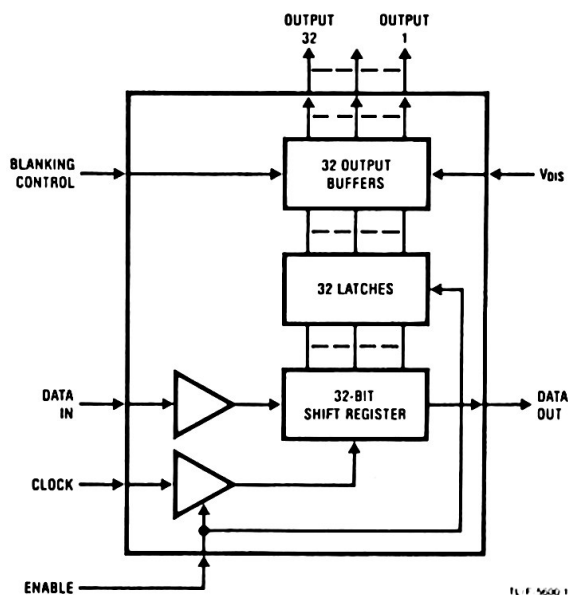


FIGURE 1

TLF 5606.1

Dual-In-Line Package

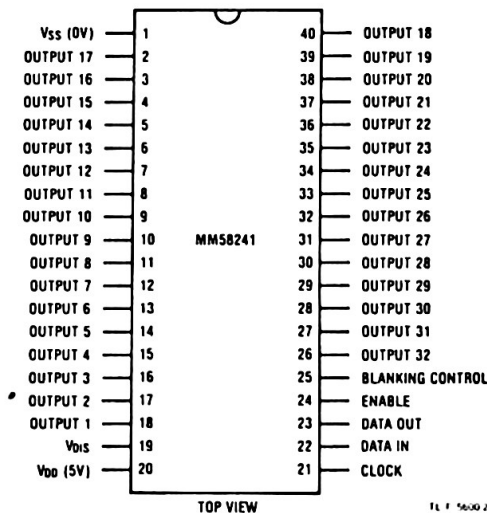


FIGURE 2

TLF 5606.2

MM58274 Microprocessor Compatible Real Time Clock

Features

- Same pin-out as MM58174A
- Timekeeping from tenths of seconds to tens of years in independently accessible registers
- Leap year register
- Hours counter programmable for 12 or 24-hour operation
- Buffered crystal frequency output in test mode for easy oscillator setting
- Data-changed flag allows simple testing for time rollover
- Independent interrupting timer with open drain output
- Fully TTL compatible
- Low power standby operation (10 μ A at 2.2V)
- Low cost 16-pin DIP

- Point of sale terminals
- Teller terminals
- Word processors
- Data logging
- Industrial process control

[illegible]

FIGURE 1

MM58341 High Voltage Display Driver

General Description

The MM58341 is a monolithic MOS integrated circuit utilizing CMOS metal gate low threshold P and N-channel devices. It is available both in 40-pin molded dual-in-line packages or as dice. The MM58341 is particularly suited for driving high voltage (35V max) vacuum fluorescent (VF) displays, (e.g., a 32-digit alphanumeric or dot matrix display).

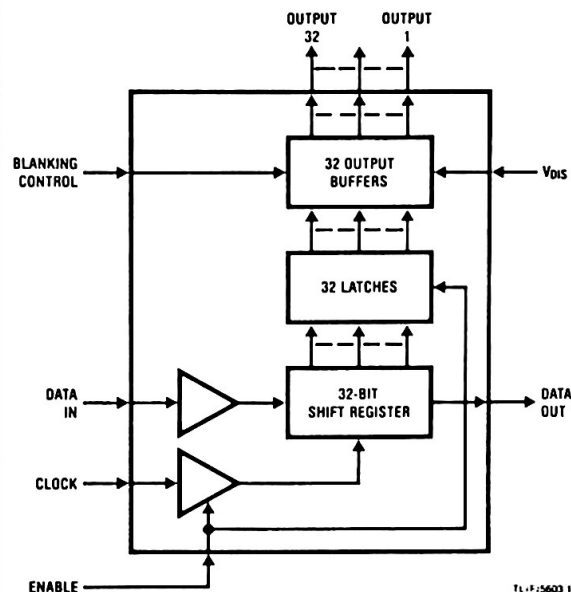
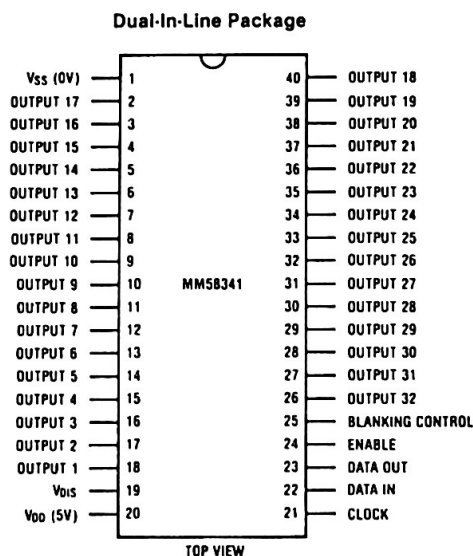
Applications

- COPS™ or microprocessor-driven displays
- Instrumentation readouts
- Industrial control indicator
- Digital clock, thermostat, counter, voltmeter
- Word processor text displays
- Automotive dashboards

Features

- Direct interface to high voltage display
- Serial data input
- No external resistors required
- Wide display power supply operation
- LSTTL compatible inputs
- Software compatible with NS display driver family
- Compatible with alphanumeric or dot matrix displays
- Display blanking control input
- Simple to cascade

Block and Connection Diagrams


FIGURE 1

FIGURE 2



NMC27C58 8,192-Bit (1024 x 8) UV Erasable CMOS PROM

General Description

The NMC27C58 is a high speed 8k UV erasable and electrically reprogrammable CMOS EPROM, ideally suited for applications where fast turnaround, pattern experimentation and low power consumption are important requirements.

The NMC27C58 is packaged in a 24-pin dual-in-line package with transparent lid. The transparent lid allows the user to expose the chip to ultraviolet light to erase the bit pattern. A new pattern can then be written into the device by following the programming procedure.

This EPROM is fabricated with the reliable, high volume, time proven, microCMOS silicon gate technology

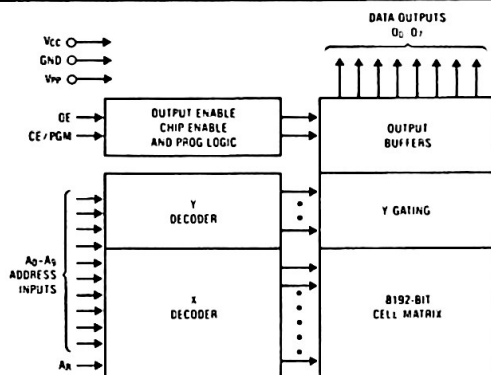
Features

- Access time -450 ns
- Low CMOS power consumption
 - Active power: 26.25 mW max
 - Standby power: 0.53 mW max (98% savings)
- Performance compatible to NSC800™ CMOS microprocessor
- Single 5V power supply
- Pin compatible to National's higher density EPROMs
- Static—no clocks required
- TTL compatible inputs/outputs
- TRI-STATE* output

Block and Connection Diagrams

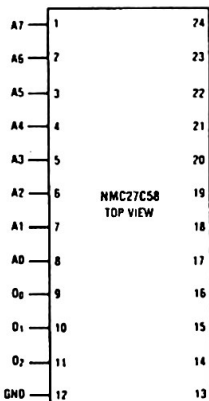
Pin Names

A0-A14	Addresses
CE	Chip Enable
OE	Output Enable
O ₀ -O ₇	Outputs
PGM	Program
NC	No Connect
*A _R	Select Reference Input Level



27C256 27256	27C128 27128	27C64 2764	27C32 2732	27C16 2716
Vpp	Vpp	Vpp		
A12	A12	A12	A7	A7
A7	A7	A7	A6	A6
A6	A6	A6	A5	A5
A5	A5	A5	A4	A4
A4	A4	A4	A3	A3
A3	A3	A3	A2	A2
A2	A2	A2	A1	A1
A1	A1	A1	A0	A0
O ₀	O ₀	O ₀	O ₀	O ₀
O ₁	O ₁	O ₁	O ₁	O ₁
O ₂	O ₂	O ₂	O ₂	O ₂
GND	GND	GND	GND	GND

Dual-In-Line Package



27C16 2716	27C32 2732	27C64 2764	27C128 27128	27C256 27256
Vcc	Vcc	Vcc	Vcc	Vcc
PGM	PGM	PGM	PGM	A14
A8	A8	A8	A13	A13
A9	A9	A9	A8	A8
Vpp	A11	A11	A9	A9
OE	OE/Vpp	OE	A11	A11
A10	A10	A10	OE	OE
CE	CE	CE	A10	A10
O ₇	O ₇	O ₇	CE	CE
O ₆	O ₆	O ₆	O ₇	O ₇
O ₅	O ₅	O ₅	O ₆	O ₆
O ₄	O ₄	O ₄	O ₅	O ₅
O ₃	O ₃	O ₃	O ₄	O ₄
O ₂	O ₂	O ₂	O ₃	O ₃

Note: National's socket compatible EPROM Connection Diagrams are shown in the blocks adjacent to the NMC27C58 pins.

*For NMC27C58A, A_R = V_{IL} for all operating modes.

*For NMC27C58B, A_R = V_{IL} for all operating modes

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NSC810A RAM-I/O-Timer

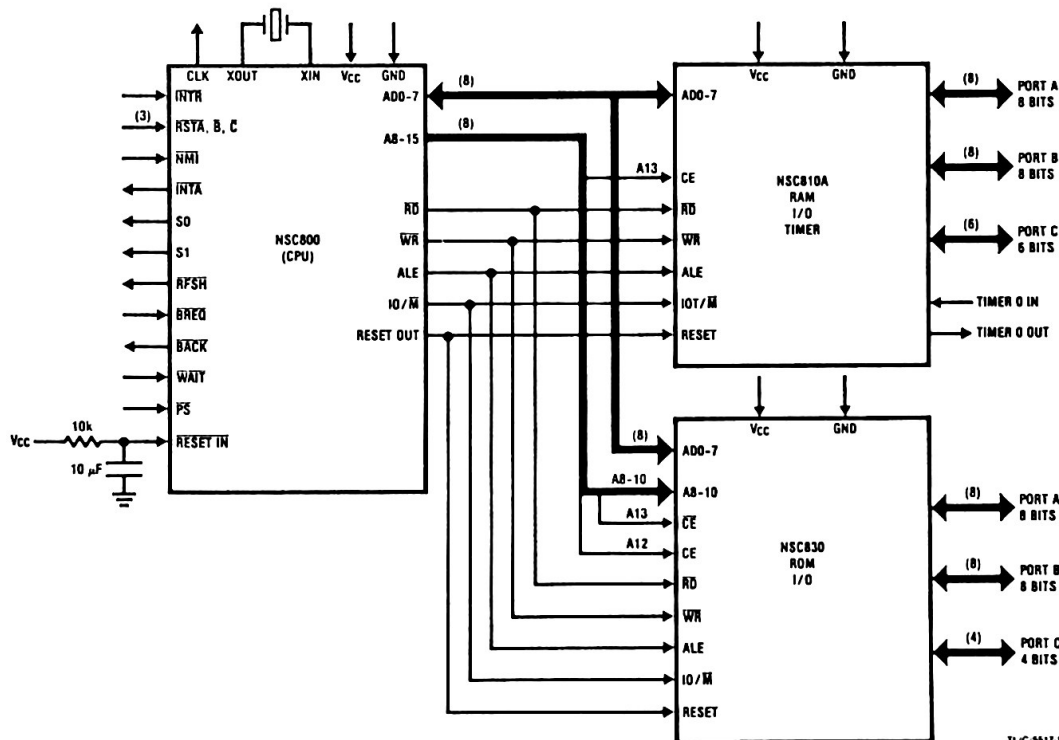
General Description

The NSC810A, which is fabricated using microCMOS silicon gate technology, functions as a memory, an input/output peripheral interface and a timing device. The memory is comprised of 1024 bits of static RAM organized as 128x8. The I/O portion consists of 22 programmable input/output bits arranged as three separate ports, with each bit individually definable as an input or output. The port bits can be set or cleared individually and can be written or read in bytes. Several types of strobed mode operations are available through port A. The timer portion of the device consists of two programmable 16-bit binary down-counters each capable of operation in any one of 6 modes. Timer counts are extendable by one of the available pre-scale values. The NSC810A comes in various speeds and package configurations, including the new high density LCC package. The NSC810A is available in full military specification 883B.

Features

- Three programmable I/O ports
- Two 16-bit programmable counter/timers
- 2.4V-6.0V power supply
- Very low power consumption
- Fully static operation
- Single-instruction I/O bit operations
- Timer operation—DC to 5 MHz
- Bus compatible with NSC800™ family
- Speed: compatible with NSC800
 - NSC810A-4—NSC800-4 @ 4.0 MHz
 - NSC810A—NSC800 @ 2.5 MHz
 - NSC810A-1—NSC800-1 @ 1.0 MHz

NSC800 Microcomputer Family Block Diagram



Programmable Array Logic Family Series 24A

General Description

The PAL* Series 24 family complements the PAL Series 20 family by providing four additional inputs, allowing more complex functions in a single package. This new family is made feasible by the new 300 mil-wide, 24-pin package.

In addition to providing more logic functions per chip, 24 pins allow for many natural functions which were previously unavailable in 20-pin packages. Examples include:

- 8-bit parallel-in parallel-out counters
- 8-bit parallel-in parallel-out shift registers
- 16-line-to-1-line multiplexers
- Dual 8-line-to-1-line multiplexers
- Quad 4-line-to-1-line multiplexers

These natural functions provide twice the density of traditional 16-pin packages.

The PAL family utilizes an advanced Schottky TTL process and the bipolar PROM fusible link technology to provide user-programmable logic for replacing conventional SSI/MSI gates and flip-flops at reduced chip count.

The family lets the systems engineer "design his own chip" by blowing fusible links to configure AND and OR gates to perform his desired logic function. Complex interconnections which previously required time-consuming layout are thus "lifted" from PC board etch and placed on silicon where they can be easily modified during prototype check-out or production. This often simplifies not only the PC board layout, but also the board itself.

The PAL transfer function is the familiar sum of products. Like the PROM, the PAL has a single array of fusible links. Unlike the PROM, the PAL is a programmable AND array driving a fixed OR array (the PROM is a fixed AND array driving a programmable OR array). In addition, the PAL provides these options:

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PAL* is a registered trademark of and used under license with Monolithic Memories, Inc.

- Variable input/output pin ratio
- Programmable TRI-STATE* outputs
- Registers with feedback

Unused inputs are tied directly to V_{CC} or GND. Product terms with all fuses blown assume the logical high state, and product terms connected to both true and complement of any single input assume the logical low state. Registers consist of D-type flip-flops which are loaded on the low-to-high transition of the clock. PAL Logic Diagrams are shown with all fuses blown, enabling the designer use of the diagrams as coding sheets.

The entire PAL family is programmed on inexpensive conventional PROM programmers with appropriate personality cards and socket adapters. Once the PAL is programmed and verified, two additional fuses may be blown to defeat verification. This feature gives the user a proprietary circuit which is very difficult to copy.

Features

- Programmable replacement for conventional TTL logic
- Reduces IC inventories substantially and simplifies their control
- Reduces chip count by 5 to 1, typically
- Expedites and simplifies prototyping and board layout
- Saves space with 300 mil-wide, 24-pin DIP packages
- Programmed on standard PROM programmers
- Programmable three-state outputs
- Last fuse reduces possibility of copying by competitors

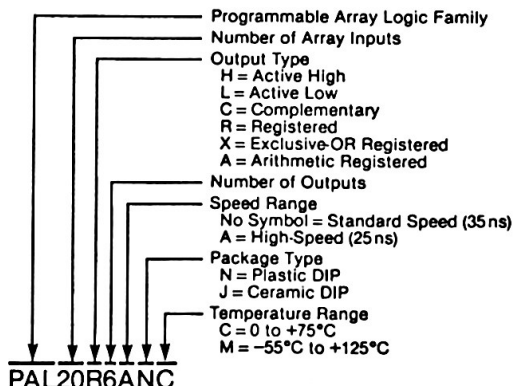
TABLE I. Part Types

Part Number	Description
PAL20L8A	OCTAL 20 Input AND-OR-INVERT Gate Array
PAL20R8A	OCTAL 20 Input Registered AND-OR Gate Array
PAL20R6A	HEX 20 Input Registered AND-OR Gate Array
PAL20R4A	QUAD 20 Input Registered AND-OR Gate Array

PAL Part Numbers

The PAL part number reveals the logic operation the part performs. The example shown, the PAL20R6ANC, is a device that accommodates 20 input terms and generates 6 register output terms. It is contained in a 24-pin plastic dual-in-line package and meets commercial temperature range specifications.

Ordering Information



Programmable Array Logic (PAL®) Low Power PAL Series 20A2

General Description

The PAL family utilizes National Semiconductor's Schottky TTL process and bipolar PROM fusible-link technology to provide user-programmable logic to replace conventional SSI/MSI gates and flip-flops. Typical chip count reduction gained by using PALs is greater than 4:1.

The family lets the systems engineer customize his chip by opening fusible links to configure AND and OR gates to perform his desired logic functions. Complex interconnections that previously required time-consuming layout are thus transferred from PC board to silicon where they can be easily modified during prototype checkout or production.

The PAL transfer function is the familiar sum of products with a single array of fusible links. Unlike the PROM, the PAL is a programmable AND array driving a fixed OR array. (The PROM is a fixed AND array driving a programmable OR array.) In addition, the PAL family offers these options:

- Variable input/output in ratio
- Programmable TRI-STATE[®] outputs
- Registers and feedback

Unused inputs are tied directly to V_{CC} or GND. Product terms with all fuses blown assume the logical high state, and product terms connected to both true and complement of any single input assume the logical low state. Registers consist of D-type flip-flops that are loaded on the low-to-high transition of the clock. PAL logic diagrams are shown with all fuses blown, enabling the designer use of the diagrams as coding sheets.

The entire PAL family is programmed on inexpensive conventional PROM programmers with appropriate personality and socket adapter cards. Once the PAL is programmed and verified, two additional fuses may be blown to defeat verification. This feature gives the user a proprietary circuit which is very difficult to copy.

Features

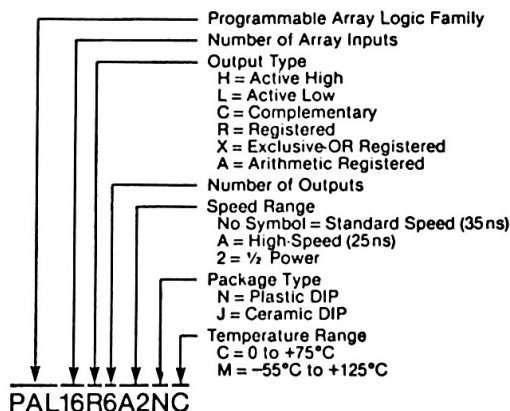
- Low power: 1/2 power of standard PAL
- Programmable replacement for TTL logic
- Simplifies prototyping and board layout
- Skinny DIP packages
- Reliable titanium-tungsten fuses
- 35ns max. propagation delay

Ordering Information

Part Number	Description
PAL16L8A2	OCTAL 16 Input AND-OR-INVERT Gate Array
PAL16R8A2	OCTAL 16 Input Registered AND-OR Gate Array
PAL16R6A2	HEX 16 Input Registered AND-OR Gate Array
PAL16R4A2	QUAD 16 Input Registered AND-OR Gate Array

PAL Part Numbers

The PAL part number reveals the logic operation the part performs. The example shown, the PAL16R6A2NC, is a device that accommodates 16 input terms and generates 6 register output terms. It is contained in a 20-pin plastic dual-in-line package and meets commercial temperature range specifications.



TLU5597-1

Programmable Array Logic (PAL®) Ultra High-Speed PAL Series 20B

General Description

The PAL family utilizes National Semiconductor's advanced oxide isolation Schottky TTL process and bipolar PROM fusible-link technology to provide user-programmable logic to replace conventional SSI/MSI gates and flip-flops. Typical chip count reduction gained by using PALs is greater than 4:1.

The family lets the systems engineer customize his chip by opening fusible links to configure AND and OR gates to perform his desired logic functions. Complex interconnections that previously required time-consuming layout are thus transferred from PC board to silicon where they can be easily modified during prototype checkout or production.

The PAL transfer function is the familiar sum of products with a single array of fusible links. Unlike the PROM, the PAL is a programmable AND array driving a fixed OR array. (The PROM is a fixed AND array driving a programmable OR array.) In addition, the PAL family offers these options:

- Variable input/output in ratio
- Programmable TRI-STATE® outputs
- Registers and feedback

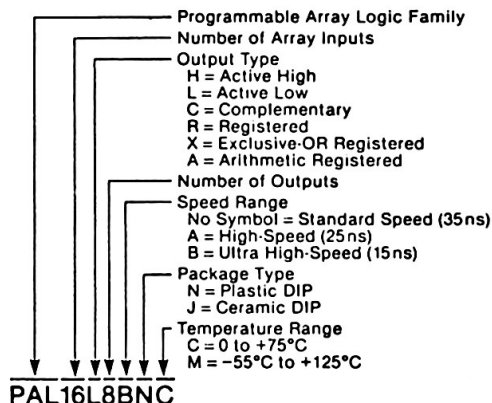
Unused inputs are tied directly to V_{CC} or GND. Product terms with all fuses blown assume the logical high state, and product terms connected to both true and complement of any single input assume the logical low state. Registers consist of D type flip-flops that are loaded on the low-to-high transition of the clock. PAL logic diagrams are shown with all fuses blown, enabling the designer use of the diagrams as coding sheets.

The entire PAL family is programmed on inexpensive conventional PROM programmers with appropriate personal-ity and socket adapter cards. Once the PAL is programmed and verified, two additional fuses may be blown to defeat verification. This feature gives the user a propri-etary circuit which is very difficult to copy.

Features

- Advanced oxide isolation process
- Programmable replacement for TTL logic
- Simplifies prototyping and board layout
- Skinny DIP packages
- Reliable titanium-tungsten fuses
- 15ns max. propagation delay

Part Number	Description	
PAL16L8B	OCTAL	16 Input AND-OR-INVERT Gate Array
PAL16R8B	OCTAL	16 Input Registered AND-OR Gate Array
PAL16R6B	HEX	16 Input Registered AND-OR Gate Array
PAL16R4B	QUAD	16 Input Registered AND-OR Gate Array



TU/L5479-1

PAL Part Numbers

The PAL part number reveals the logic operation the part performs. The example shown, the PAL16L8BNC, is a device that accommodates 16 input terms and gener-

ates 8 active-low output terms. It is contained in a 20-pin plastic dual-in-line package and meets commercial temperature range specifications.

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SCX6260 CMOS Gate Array

General Description

This 6000 gate array with sub-nano-second performance is manufactured using National Semiconductor's microCMOS process with 2 micron feature sizes. The high performance SCX6260 contains three major sections:

Internal Matrix: 3953 cells, organized as 59 columns by 67 rows, consisting of 3 transistor pairs each, equivalent to 5930 2-input gates ($1\frac{1}{2}$ gates per cell).

I/O Circuitry: Out of 172 pads, 12 are used for power supply, 88 are bidirectional and 66 can be used as inputs only. Four are dedicated to test, 1 is a clock pin and 1 an output disable.

On-Chip Maintenance System: For an increase in die area of only 12%, a powerful test system, equivalent to 2500 gates, can be implemented. Only 4 pins, system clock, and power are needed to test the entire matrix, self-test routines can be applied, and since the I/O levels can be controlled, AC and DC parameters can be measured easily.

Features

- Manufactured in microCMOS (dual metal, silicon gate)
- 2μ feature size, 0.85 ns typical gate delay (2-input NAND with 2 loads plus 100 mils of interconnect metal)
- Complexity: 6K gates in matrix plus 2.5K in I/Os and test circuitry
- Packages: 124 and 172 pins; PGA, LCC, LDCC and PCC
- I/O count: 66 input pads
88 bidirectional
- All inputs can be defined CMOS- or TTL-compatible, all outputs have TTL- and CMOS drive capability
- Output buffers: 6mA min, 12mA typical drive capability
- Operating range: $5V \pm 10\%$, $0-70^\circ C$
- Powerful on-chip test circuitry (OCMS—On-chip Maintenance System)
- Extensive macro library: 66 internal macros, 8 others (I/Os and OCMS)
- Dynamic macros for high density and speed
- Stackable macros for maximum efficiency
- Alternate source
- Design software for leading workstations

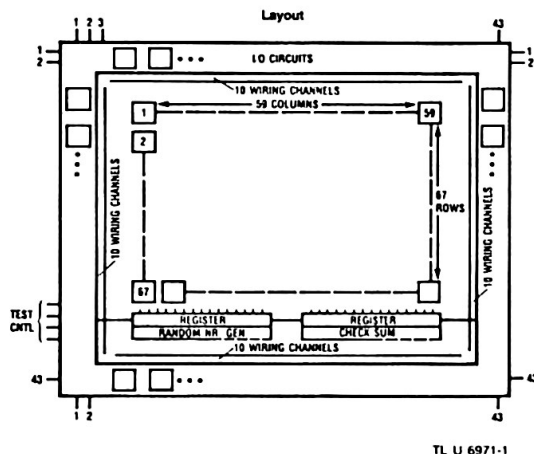


FIGURE 1. Layout of the SCX6260

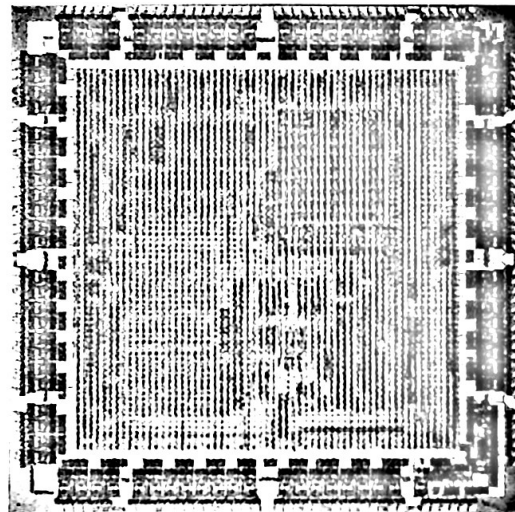
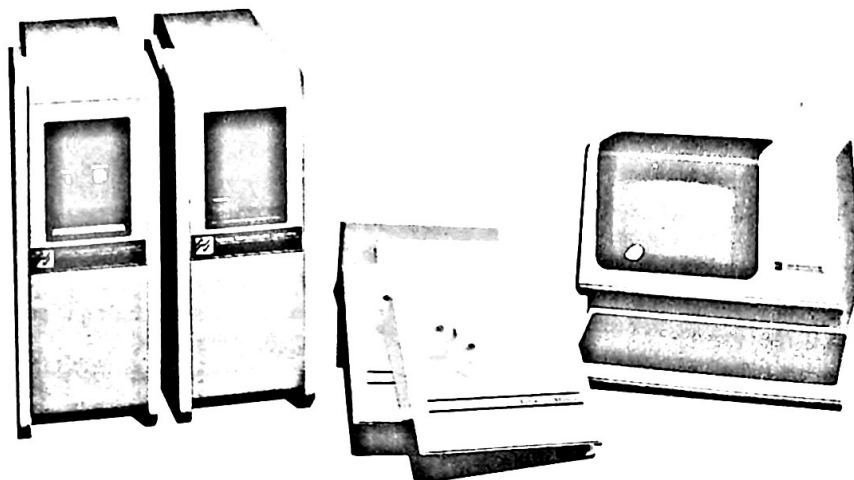


FIGURE 2. Die Photo of the SCX6260

SYS 32™ Multi-User Development System for the Series 32000™ Microprocessor Family



- **GENIX™** a derivative of Berkeley 4.1 bsd UNIX™ operating system
- Time-shared support for up to eight users
- Series 32016 Microprocessor based
- Demand-Paged Virtual Memory support
- Easy to use, proven programming environment
- 1.25 Megabytes RAM, expandable to 3.25 Megabytes
- 20 Megabytes Hard Disk, expandable to 140 Megabytes
- Streamer Tape backup, with 20 Megabyte cartridges
- C and Pascal High Level Language Compilers
- Series 32000 assembler
- Supports emulation of Series 32000 Microprocessor Family

Product Overview

The SYS32 is a multi-user development system that provides powerful software and hardware tools for the development of applications using National Semiconductor's Series 32000 Microprocessor Family components.

Based on the Series 32016 16-Bit Microprocessor, SYS32 gives the designer access to an assembler, high level language compilers, and real-time In-System Emulation (ISE™) tools. Total development support is provided for up to eight time-sharing users.

The SYS32 includes two main modules: the Processor module, which houses most of the electronics and the Disk-Tape module, which houses the hard disk and streamer tape back-up.

Optional disk drive modules may be added to increase hard disk capacity. Disk drive modules contain two drives of 20 Megabytes each, for a total of 40 Megabytes per module.

One terminal is provided with the system. Additional terminals may be added to the system as the demand warrants. Emulation and software development work may be performed concurrently. Shared resources of the hard disk and user-supplied printer lowers the system's cost per user.

National's GENIX Operating System is an enhanced version of Berkeley 4.1 bsd UNIX. These enhancements fully utilize the advanced architecture of the Series 32000 Microprocessor Family.

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UNIX™ is a trademark of Bell Laboratories

Circle DATA UPDATE No. 113645

TP3064, TP3067 Monolithic Serial Interface CMOS CODEC/FILTER Combos

General Description

The TP3064 (μ -law) and TP3067 (A-law) are monolithic PCM CODEC/FILTERS utilizing the A/D and D/A conversion architecture shown in Figure 1, and a serial PCM interface. The devices are fabricated using National's advanced double-poly CMOS process (microCMOS).

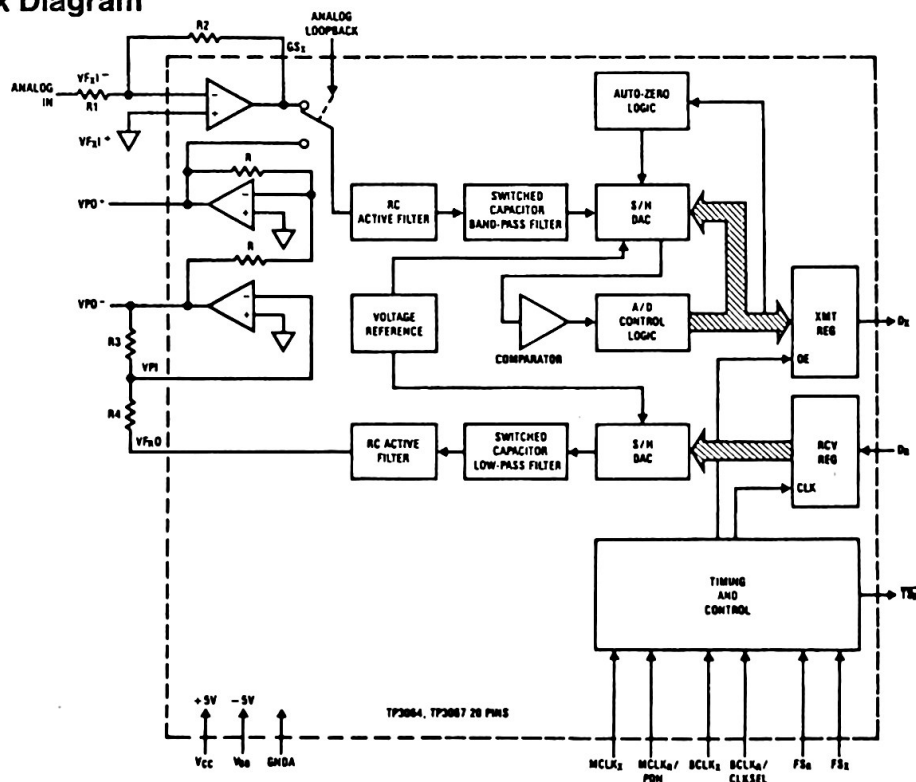
Similar to the TP3050 family, these devices feature an additional Receive Power Amplifier to provide push-pull balanced output drive capability. The receive gain can be adjusted by means of two external resistors for an output level of up to $\pm 6.6V$ across a balanced 600Ω load.

Also included is an Analog Loopback switch and \overline{TS}_X output.

Features

- Complete CODEC and filtering system including:
 - Transmit high-pass and low-pass filtering
 - Receive low-pass filter with $\sin x/x$ correction
 - Active RC noise filters
 - μ -law or A-law compatible CODEC and DECODEC
 - Internal precision voltage reference
 - Serial I/O interface
 - Internal auto-zero circuitry
 - Receive push-pull power amplifiers
- μ -law—TP3064
- A-law—TP3067
- Meets or exceeds all D3/D4 and CCITT specifications
- $\pm 5V$ operation
- Low operating power—typically 70 mW
- Power-down standby mode—typically 3 mW
- Automatic power-down
- TTL or CMOS compatible digital interfaces
- Maximizes line interface card circuit density

Block Diagram



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